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Issue 11/2008

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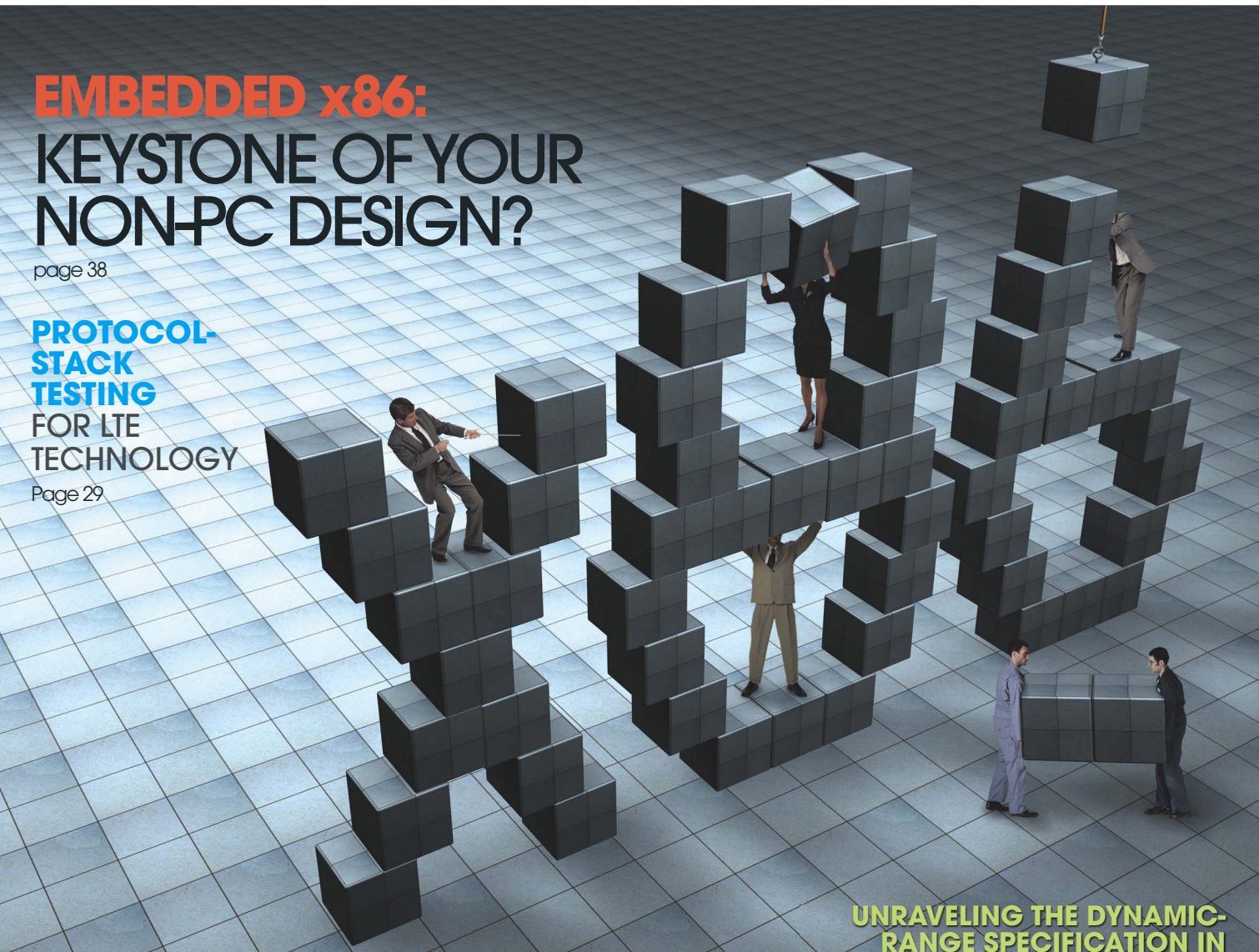
EMBEDDED x86: KEYSTONE OF YOUR NON-PC DESIGN?

page 38

PROTOCOL-STACK TESTING FOR LTE TECHNOLOGY

Page 29



UNRAVELING THE DYNAMIC-RANGE SPECIFICATION IN MODERN SPECTRUM ANALYZERS

Page 49

MULTICORE-PROGRAMMING FRAMEWORKS FOR EMBEDDED-MULTIMEDIA APPLICATIONS

Page 57

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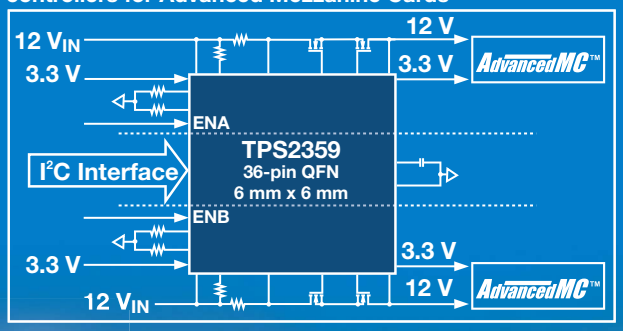

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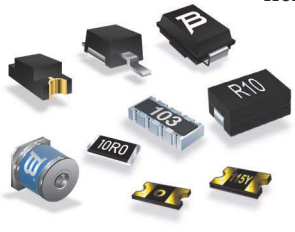

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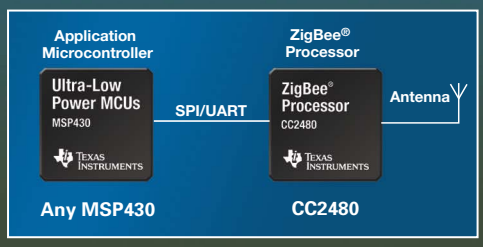

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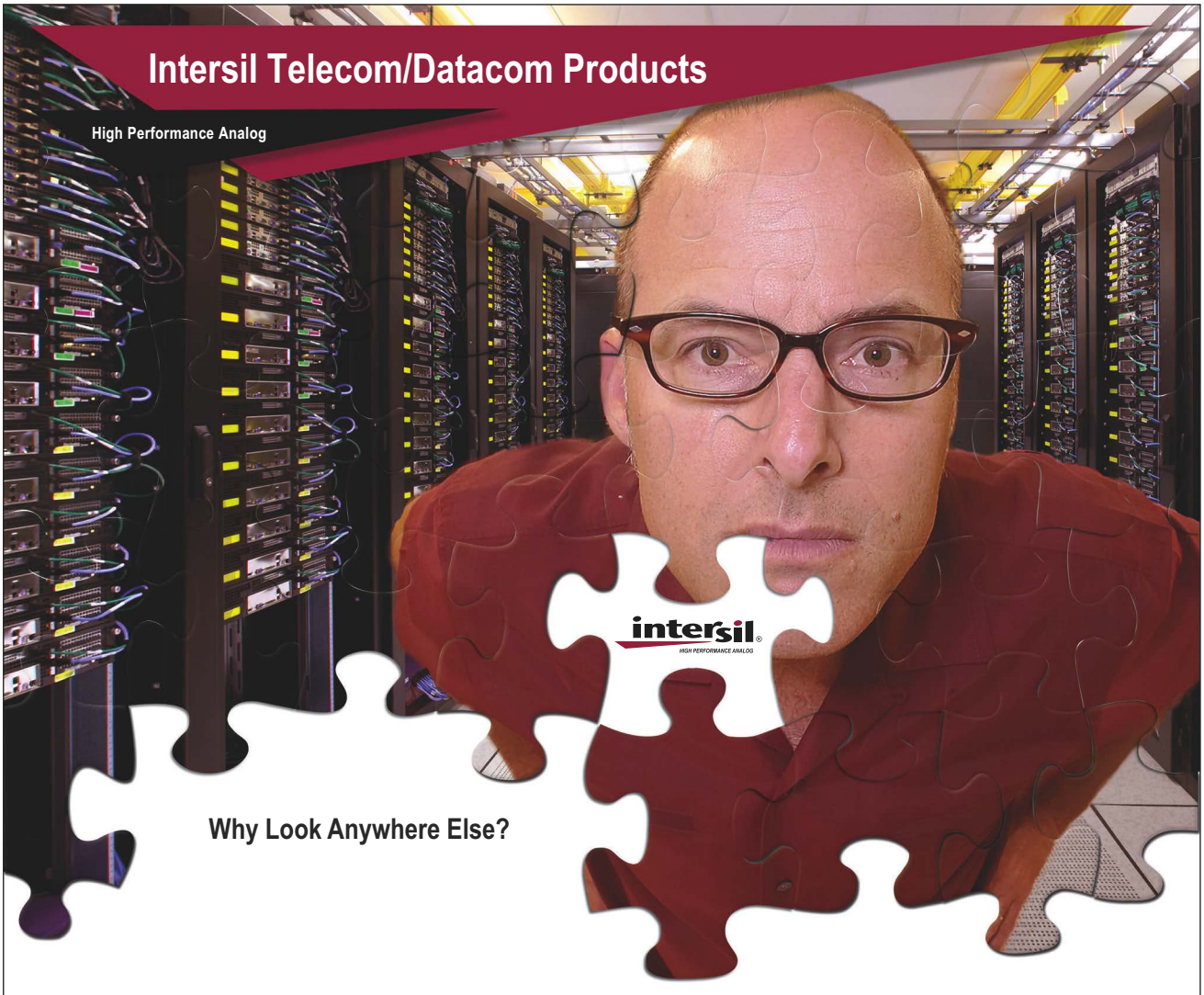

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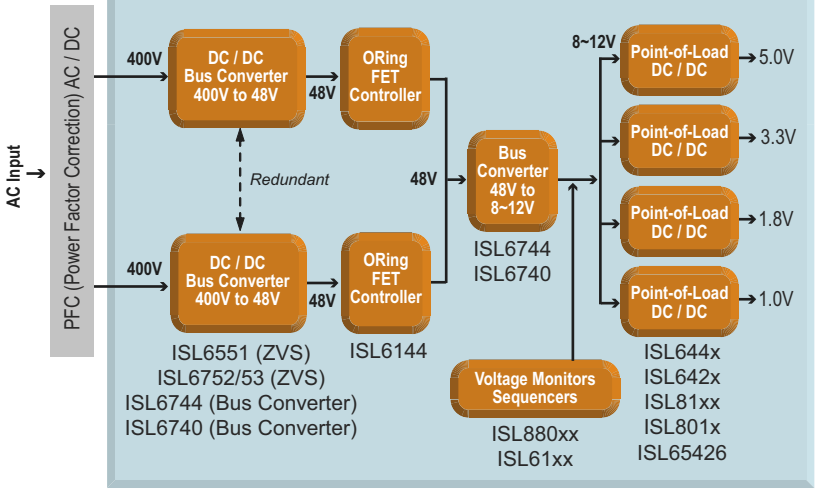

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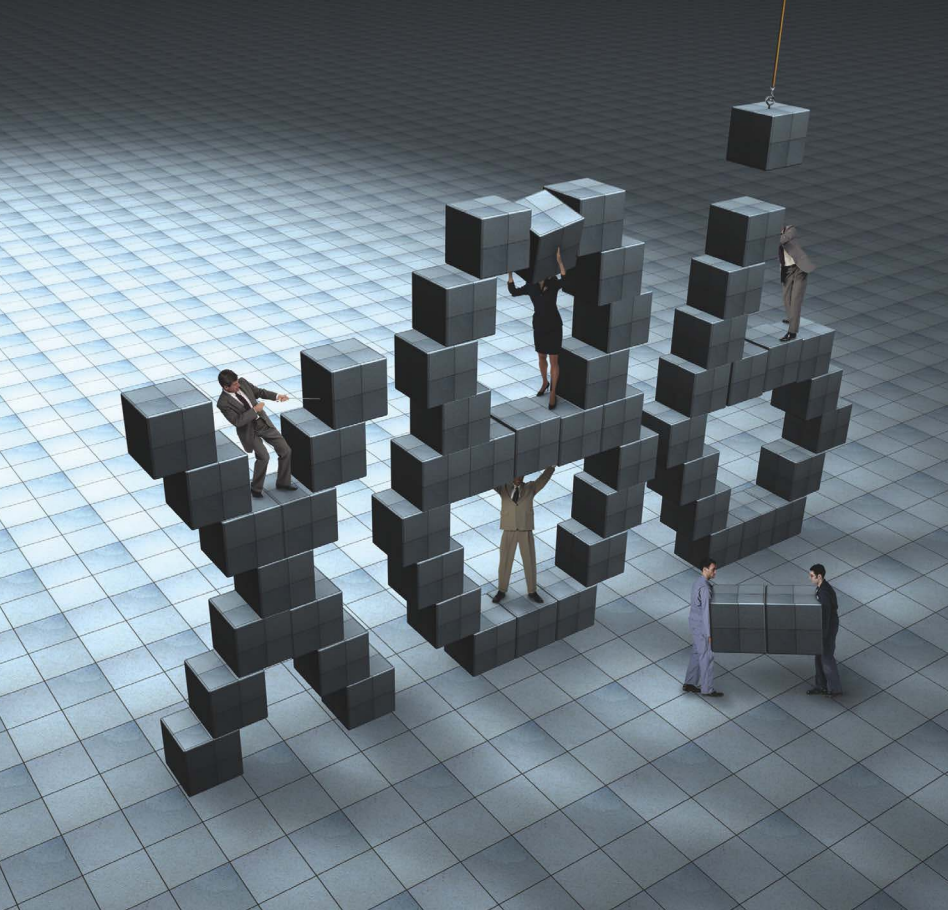


EDN contents

5.29.08

Unraveling the dynamic-range specification in modern spectrum analyzers

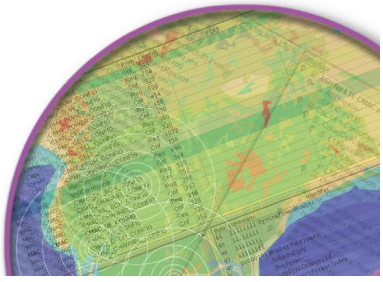
by Satish Dhanasekaran and Darrin Russell, Agilent Technologies

Multicore-programming frameworks for embedded-multimedia applications

by Kaushal Sanghai, Rick Gentile, and David Katz, Analog Devices

Embedded x86: keystone of your non-PC design?

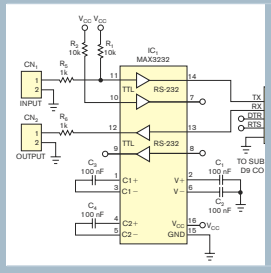
 by Brian Dipert, Senior Technical Editor



Protocol-stack testing for LTE technology

by Christina Gessner, Rohde & Schwarz

DESIGNIDEAS



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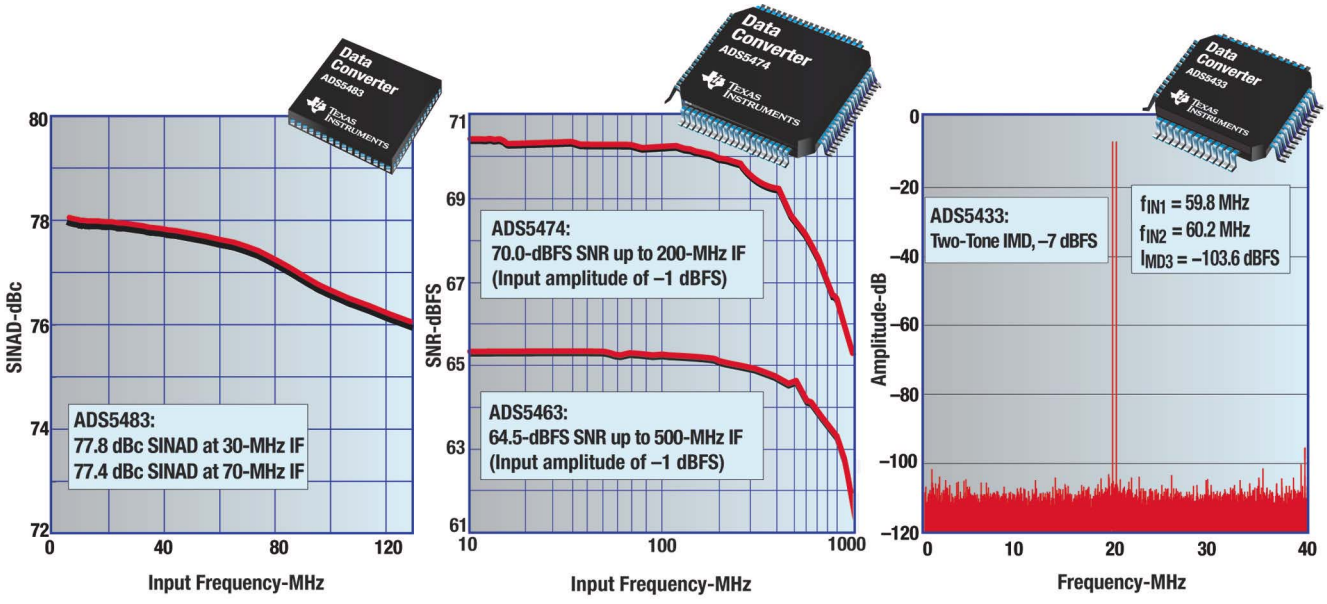

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contents 5.29.08

pulse

Dilbert 16

18

82

86

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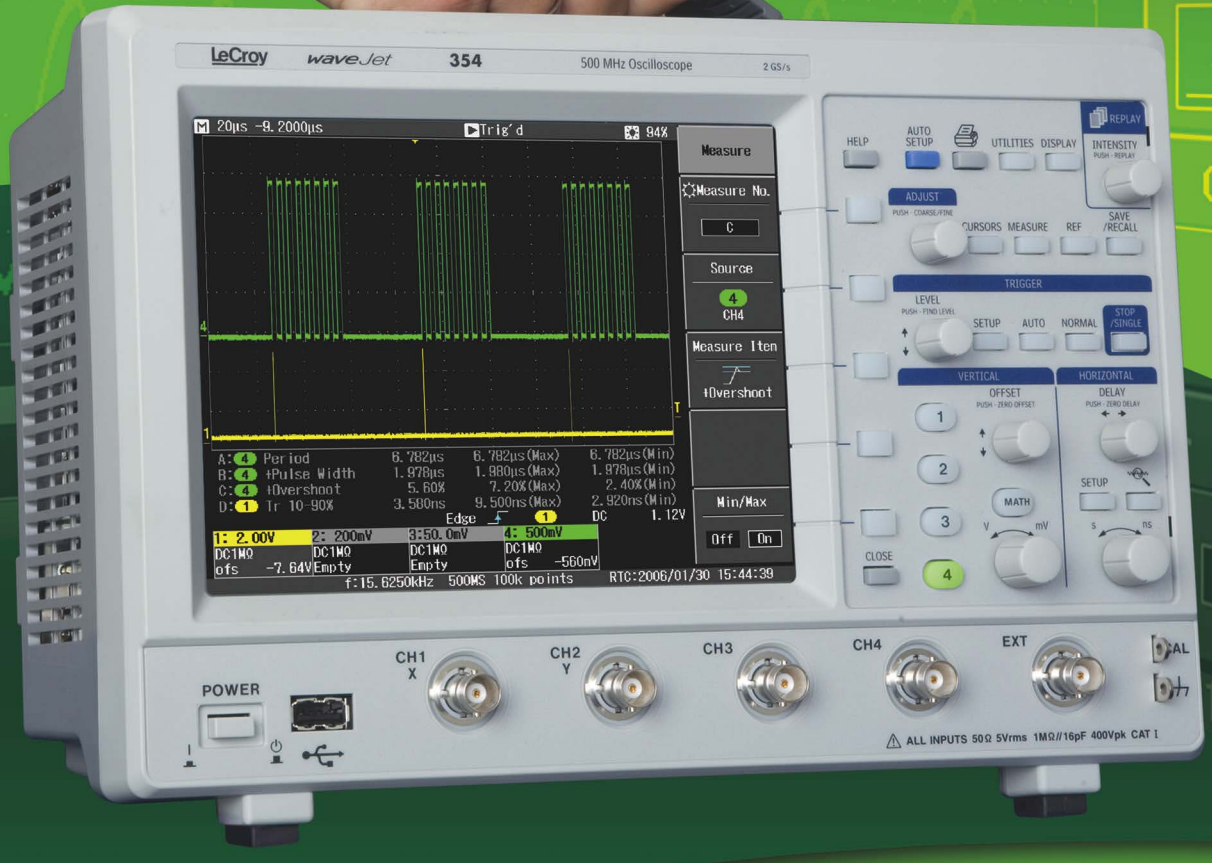

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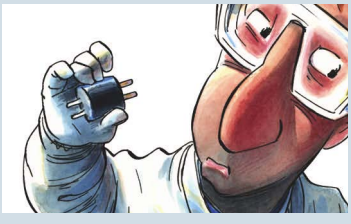

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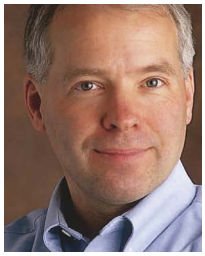

BY RICK NELSON, EDITOR-IN-CHIEF

Consumer electronics: too daunting for our addled brains?

It's no secret that consumer spending has been driving the economy, and high-tech company Credence Systems has retooled its businesses to focus on consumer electronics (**Reference 1**). But it's now questionable whether consumers will continue their spending, despite income-tax rebates that some of you may have received by now. At bloomberg.com (**Reference 2**), economist Ken Goldstein said, "Consumers have gone into the bunkers. [They] fear that their budgets are getting squeezed tighter and tighter. … A $600 check isn't enough to turn things around."

But it may be more than a weak economy that drives consumers away from electronic products. They seem not to want much of what they can afford. That's the conclusion I reached after reading an article in *The Wall Street Journal* that cites a study by Accenture noting that the US electronics industry last year spent about $13.8 billion handling returned products (**Reference 3**). The article states, "Especially galling to manufacturers is that many returns are preventable: Only about 5% of returns were because a product was truly defective." Many devices were returned simply because they were too confusing to use.

My conclusion: If you make a product with a user interface so poor that the average consumer can't figure it out, then your product is defective, even if all the transistors, buttons, displays, and other components work.

And if it does turn out that consumers—at least young consumers—aren't smart enough to understand and appreciate the latest high-tech gadgets, the consumer-electronics industry may have only itself to blame. You might infer this conclusion from Mark Bauerlein's new book, *The Dumbest Generation: How the Digital Age Stupefies Young Americans and Jeopardizes Our Future*.

If the average consumer can't figure it out, then your product is defective.

The book, slated for a May 15 release, was not available at press time, but in commentary on boston.com, Bauerlein notes that young people don't read books; they spend their time and money on *Grand Theft Auto* instead (**Reference 4**). The predominance of video use, Bauerlein adds, makes schoolwork suffer. Boston.com reinforces this point by citing a *Boston Globe* article noting that "thousands of Massachusetts public school graduates are ending up in remedial reading and writing classes in college."

Bauerlein also says that spelling is a lost art, thanks to instant messaging. And so is composition. He adds, "On *MySpace*, if you write clearly and compose coherent paragraphs with informed observations on history and current events, 'buddies' will make fun of you." In short, concludes Bauerlein, "Kids are drowning in teen stuff delivered 24/7 by the tools, and adult realities can't penetrate."

It all has a nice symmetry: The consumer-electronics industry fries our brains, so we are too stupid to be able to set up and operate consumer electronics.

And this situation can have a deleterious effect on the engineering profession. As I've noted before, entry-level engineers are often more adept at playing video games than at working in a real-world laboratory (**Reference 5**).EDN

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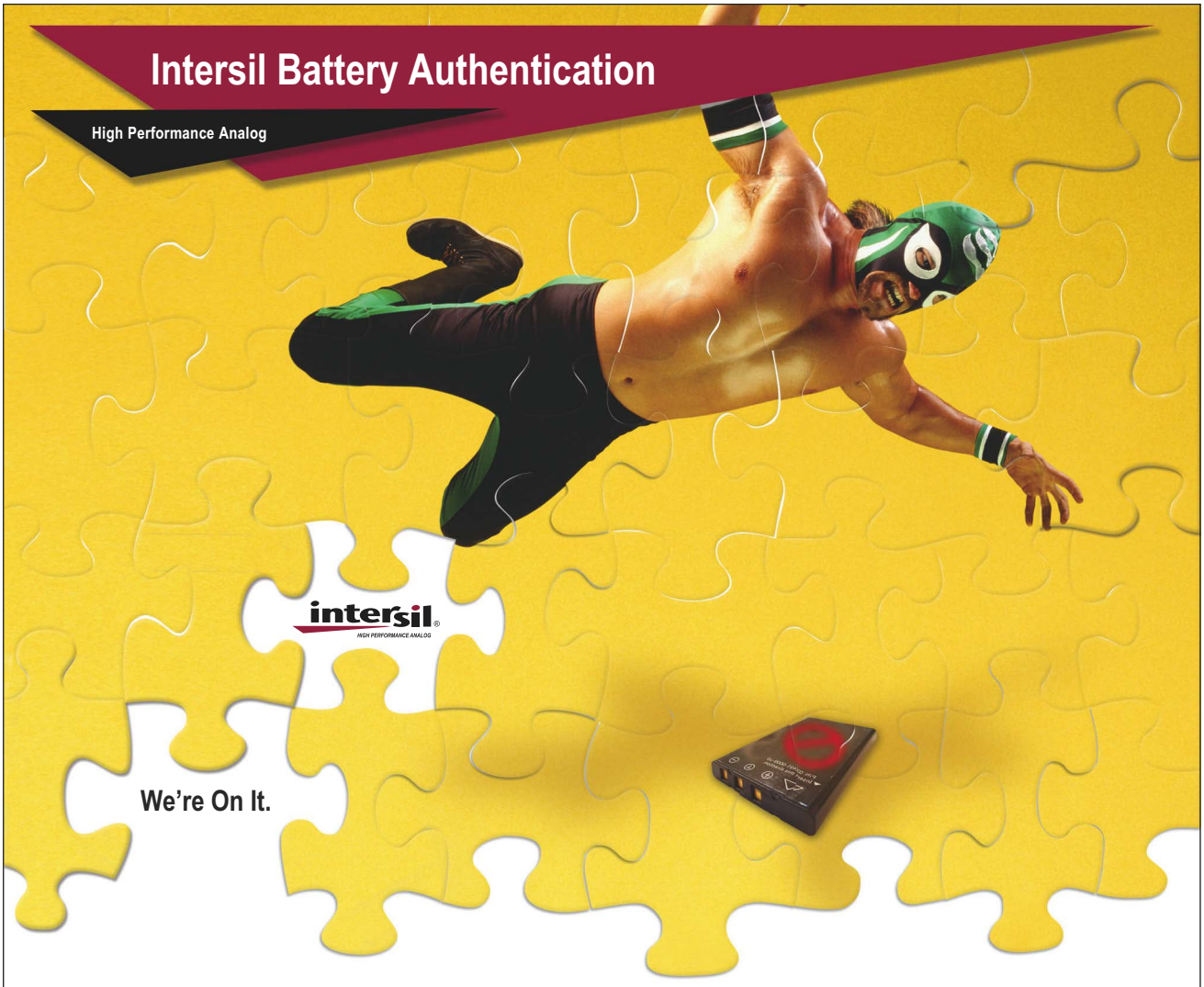

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- FlexiHash+ engine uses two sets of 32-bit secrets for authentication code generation.
- 16x8 one-time programmable ROM memory.
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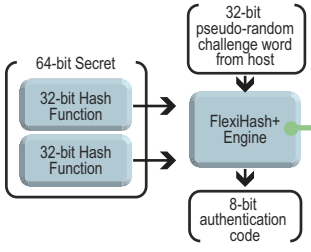
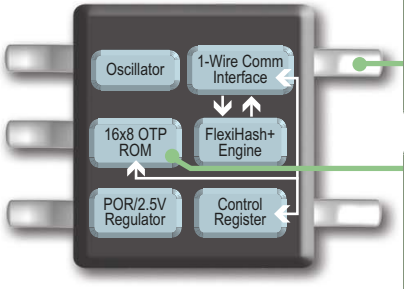


Patent pending FlexiHash+ engine consists of four separate programmable CRC calculators. Two sets of 32-bit secret codes are used for authentication code generation.



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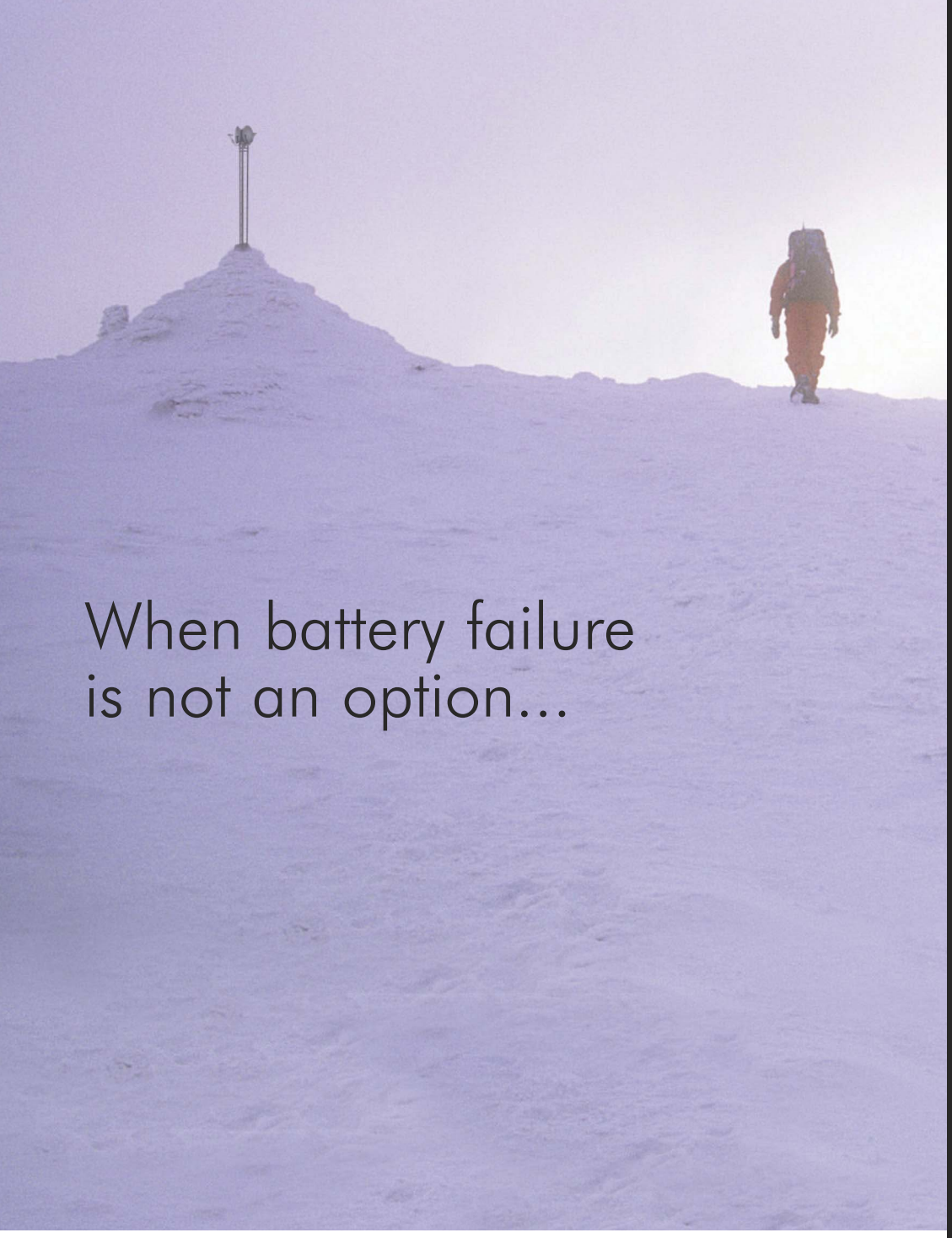

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Pentek shrinks software-radio module

At the recent Critical Embedded Systems conference in Scottsdale, AZ, Pentek introduced its latest high-performance, high-resolution software-radio module. The Model 7151 PMC (peripheral-component-interconnect-mezzanine card) features four 200-MHz, 16-bit ADCs that feed a proprietary FPGA-IP (intellectual-property) core to deliver 256 channels of digital downconversion. With independent frequency tuning for each channel, the Model 7151 can downconvert any signal within any of the four digitized 100-MHz input bands, making it ideal for GSM (global-system-for-mobile)-communication cell-phone monitoring and signal-intelligence applications.

The device comes in four banks of 64 digital-downconversion channels; you can configure each bank for a unique output-signal bandwidth to accommodate applications requiring mixed-signal types or multiple modulation schemes. You can independently source each bank from any one of the four ADCs, which you typically assign to specific antennas. Software drivers are available for the device, which comes ready to use with developed and installed FPGA code. Software and software-support packages are available for the Linux, Windows, and VxWorks operating systems. The Model 7151 PMC-module version is available for $14,500, with delivery in 10 to 12 weeks.**—by Warren Webb**

▷**Pentek**, www.pentek.com.

▷**Critical Embedded Systems**, www.critical-embedded-systems.com.

The Model 7151 contains a complete software-radio system on a single PMC module with 256 digital-downconversion channels and four 200-MHz, 16-bit ADCs.

NXP opts for soft encryption

NXP has announced that it will incorporate NTRU's software-based encryption in NXP's ARM7 (www.arm.com)-based microcontrollers. The software-based product will allow you to upgrade a microcontroller in an installed application. NXP will supply the NTRU algorithms as security libraries for its microcontrollers, providing standard features, such as encryption, decryption, digital signatures, RNG (random-number generation), and key negotiation. These features will establish confidentiality, authentication, and integrity in transactions. The available hash algorithms include SHA (secure hashing algorithm) 1, MD5 (message digest 5) and X9.82 RNG, AES (Advanced Encryption Standard), triple-DES (Data Encryption Standard), RSA (Rivest/Shamir/Adleman), DSA (digital-signature algorithm), and Diffie-Hellman. Pricing will be on a royalty basis.

In opting for a software approach for security, an NXP spokesman explains, a key factor was flexibility and the option of upgrading or retrofitting designs with intersystem data security. The approach has a typical flash-code overhead of approximately 12 kbytes, and it will typically employ about 10% of the computing resources of the company's LPC 2400 device. With the software option, you can change algorithms while the system is in use, either as a result of the compromising of an algorithm or as a matter of routine. You can also manufacture your product anywhere, with no export-license conditions until you load the software onto the system. To configure the security technology, designers license the code directly from NTRU; the technology runs only on NXP's ARM chips.

—by Graham Prophet

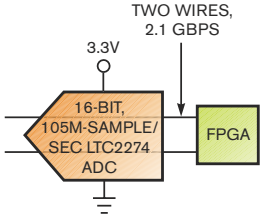
▷**NXP Semiconductors**, www.nxp.com.

▷**NTRU**, www.ntru.com.

16-bit, 105M-sample/sec serial-output ADC has two-wire data stream

Linear Technology Corp's new, 16-bit, 105M-sample/sec LTC2274 ADC has a two-wire serial interface, which greatly reduces the number of data lines between the ADC and the FPGA. The data interface is a single self-clocking, differential pair communicating at 2.1 Gbps using 8B/10B encoding. The LTC2274 serial output is compatible with many high-speed-FPGA interfaces, including Xilinx's (www.xilinx.com) Rocket IO, Altera's (www.altera.com) Stratix II GX I/O, and Lattice Semiconductor's (www.latticesemi.com) ECP2M I/O.

The part is suitable for communications systems, including cellular base stations, WiMax (worldwide interoperability for microwave access), WCDMA (wideband-code-division multiple access), TDSCDMA (time-division-synchronous CDMA), and multicarrier GSM (global-system-for-mobile) communication. It also finds use in multichannel ADC systems in ATE (automatic-test equipment), medical imaging, and instrumentation. The device comes in a 6×6-mm QFN-40 package, whose size makes the part useful in space-constrained data-acquisition systems.



The LTC2274 uses a two-wire data interface that uses 30 fewer pins than a parallel-LVDS (low-voltage-differential-signaling) device.

The LTC2274 provides an internal transparent-dither circuit that improves the ADC's SFDR (spurious-free-dynamic-range) response to beyond 100 dBc for low-level input signals. A user can enable an optional data scrambler to randomize the spectrum of the serial link, reducing interference from the serial-digital outputs. A programmable-gain amplifier in the front end allows either a 2.25 or a 1.5V p-p input range. The part outputs data in two's complement or offset-binary formats. The device has separate shutdown pins for the analog and the digital sections to conserve power. An on-chip duty-cycle-stabilizer circuit facilitates non-50%-clock-duty cycles.

The LTC2274's ac specifications include a 77.5-dBFS (decibels relative to full-scale) SNR (signal-to-noise ratio), a 77.8-dBFS noise floor, and a 100-dB SFDR at baseband. The sample-and-hold section has a 700-MHz full-power bandwidth. The part exhibits 80-fsec-rms jitter, which enables undersampling performance of input frequencies as high as 500 MHz. The LTC2274 consumes 1.3W from a 3.3V analog supply.

> The device has separate shutdown pins for the analog and the digital sections to conserve power.

The company plans this summer to release pin-compatible 80M- and 65M-sample/sec versions. Linear can screen products to order at sampling rates higher than the rated data-sheet specifications. The LTC2274 sells for $68 (1000). Production quantities will be available in July in both commercial- and industrial-temperature grades. Demonstration boards and samples are available online now.—**by Paul Rako**

▷**Linear Technology Corp**, www.linear.com/2274.

IMEMS SENSOR DETECTS IRREGULARITIES

Analog Devices' ADXL001 vibration and shock sensor allows designers of industrial equipment or instrumentation to cost-effectively incorporate continuous, high-performance, high-bandwidth vibration monitoring into their designs. The single-chip, 5×5-mm iMEMS (integrated microelectromechanical-system) package fits into motor-control circuitry or mounts on factory equipment. The chip comes in full-scale dynamic ranges of ±70, ±250, and ±500g, with a 22-kHz resonant frequency, a frequency response down to dc, and nonlinearity of 0.2% of full-scale range.

The chip requires no calibration and works with Analog's SigmaDSP processor and SigmaStudio GUI. It has an extended industrial-temperature range of −40 to +125°C. Input voltage is 3.3 to 5V. The ADXL001 sells for $35 (1000) and comes in an eight-pin LCC ceramic package.

—by Margery Conner

▶**Analog Devices, www.analog.com.**

The factory-calibrated ADXL001 iMEMS vibration sensor provides early detection of motor-bearing vibration to 22 kHz.

DILBERT By Scott Adams

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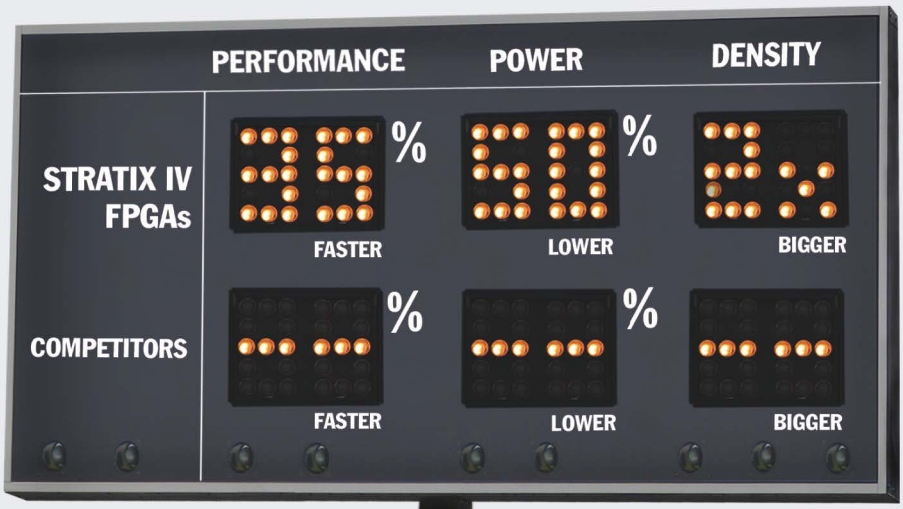

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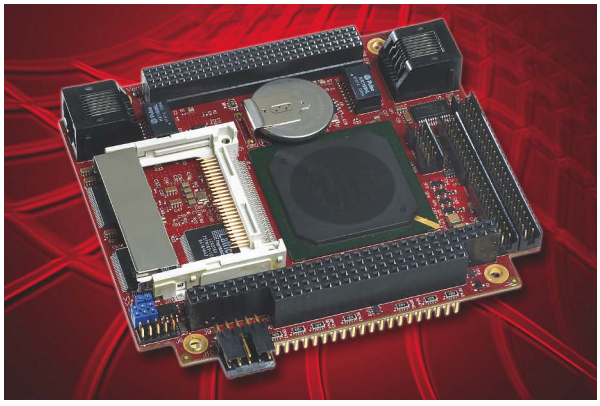
Cougar computer attacks rugged applications

With an eye toward demanding military, aerospace, medical, and industrial applications, VersaLogic announced the Cougar single-board computer at the April Embedded Systems Conference. The new PC/104-plus board offers designers of ruggedized systems the benefits of fanless operation, soldered-on system memory, and −40 to +85°C extended-temperature operation. The Cougar's AMD (www.amd.com) LX 800 processor delivers Celeron 800-MHz-equivalent performance while drawing less than 5W of power. Standard onboard features include 256 Mbytes of SDRAM, dual 10/100-Mbps Ethernet, four USB 2.0 ports, an IDE (integrated-drive-electronics) interface, and three communications ports. A CompactFlash socket provides high-capacity, onboard storage with no moving parts. USB ports provide options for keyboard, mouse, external storage, and other devices.



The Cougar PC/104-plus single-board computer features fanless operation, soldered-on system memory, and extended-temperature operation while drawing less than 5W of power.

The board integrates flat-panel support with MMX (multimedia extensions) and 3DNow! extensions for video-intensive applications. The PC/104-plus interface supports both ISA (industry-standard-architecture) and PCI (peripheral-component-interconnect) add-on modules. Standard pass-through connectors allow the board to reside either above or below other PC/104 modules. The Cougar is compatible with a variety of popular operating systems, including Windows, QNX, VxWorks, and Linux. It sells for approximately $795 (OEM quantities).

—by Warren Webb

▷**VersaLogic Corp**, www.versalogic.com.

MICROCONTROLLER DRAINS BATTERIES DOWN TO 0.9V

Silicon Laboratories based its new C8051F9xx line of 8-bit microcontrollers on a new version of the Intel (www.intel.com) 8051 core, which its designers recast as a pipelined, 100-MIPS CPU. The company adds mixed-signal and analog features, such as high-precision data converters. The new parts operate at voltages as low as 0.9V to extract the greatest possible life from a single-cell battery. The devices have onboard boost converters that can supply the microcontroller and as much as 65 mW of power for external circuitry, which allows you to use power from a primary cell until the battery drains at 0.9V.

However, Silicon Labs says that this architecture allows a wide range of efficient battery-operation modes that go beyond simply draining a single cell to its limits. It operates from 0.9 to 3.6V and incorporates a low-drop-out regulator. You can power the device from two cells in series, and the regulator delivers a constant 1.7V to the core. Alternatively, you can use two cells in parallel and exploit the boost converter to operate down to their limits. Either way, the company claims, the configurations to power the chip are more energy-efficient than other devices currently in the market. A graphical/spreadsheet-design tool estimates battery life in the various configurations, taking into account the discharge characteristics of different cell chemistries. As a primary cell drops close to 0.9V, its remaining capacity is limited, and, at that point, the boost converter makes maximum demands on it, so it may quickly reach its end of life.

In a design with a separate dc/dc converter and microcontroller, the converter must run continuously even if the microcontroller is in sleep mode. In the C8051F9xx, a separate power path allows the converter to be off while the core is in sleep mode, saving power. The C8051F9xx has a typical sleep-mode current of less than 50 nA. The microcontroller can wake up from its low-power sleep mode with the CPU operating at 25 MIPS and can make an analog-to-digital conversion in 2 μsec. In active mode, current demand is 170 μA/MHz. On-chip features include 64 kbytes of flash and 4 kbytes of RAM; a 10-bit, 300k-sample/sec ADC with an internal fast-wake-up-voltage reference; a timing module; and internal oscillators.

Silicon Labs provides an integrated development environment, a target board, cables, and a power supply in a starter kit, or you can begin evaluation using an inexpensive ToolStick daughtercard and base adapter. The chips are in 24-pin, 4×4-mm QFN; 5×5-mm, 32-pin QFN; and 7×7-mm, 32-pin LQFP packages, with prices starting at $1.99 (10,000). Development kits cost $99, and ToolStick daughtercards cost $17.90.—by Graham Prophet

▶**Silicon Labs**, www.silabs.com.

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ANALOG DEVICES

IMEC, Renesas research reconfigurable RF transceivers

To perform research on 45-nm RF transceivers targeting 1-Gbps cognitive radios, semiconductor supplier Renesas Technology Corp has entered a strategic research collaboration with the IMEC (Interuniversity Microelectronics Center) nanoelectronics and nanotechnology research center's SDR (software-defined-radio)-front-end program. This research includes reconfigurable RF products; high-speed, low-power ADCs; and new approaches to digitizing future RF architectures. To bolster development of future mobile-electronics products, Renesas will place researchers onsite at IMEC.

IMEC's SDR-front-end program targets the development of a new generation of cost-, performance-, and power-competitive reconfigurable radios in 45-nm-digital-CMOS technology, which will contain a programmable center frequency of 100 MHz to 6 GHz and programmable bandwidth of 100 kHz to 40 MHz to cover key communication standards, with a merit comparable to state-of-the-art single-mode transceivers.

The IMEC research program builds on its previous 130-nm RF-transceiver results, including a prototype of a true SDR-transceiver IC. The collaborators will also develop further evolutions of IMEC's ADCs.

"The ability to develop an innovative RF architecture with scaled-down CMOS technology and circuit technologies in transceiver products supporting next-generation cellular standards, such as 3GPP-LTE and 4G, is one of the key differentiators for our products that are superior in cost advantages, performance, and power," says Masao Nakaya, board director and executive general manager of the LSI (large-scale-integration)-product technology unit at Renesas.

—by Ann Steffora Mutschler

▷**Renesas**, www.renesas.com.

▷**Interuniversity Microelectronics Center**, www.imec.be.

FPGAs target power-constrained designs

Actel has extended its Igloo series of low-power FPGAs with Igloo Plus. Whereas the company designed the original devices for maximum density, it optimized the new parts for I/O count. The core-logic structures remain the same as in the earlier parts. The three-device family spans 30,000 to 125,000 gates with 120, 157, or 212 I/Os. They have as much as 64% more I/Os per equivalent device than the earlier parts, arranged in four banks.

You can hot-swap the connections, which have Schmitt-trigger inputs for noise tolerance. As with the Igloo series, they support Actel's Flash Freeze feature, which allows you to place the device in a very-low-power standby mode that nevertheless holds I/O states and from which the device can wake in 1 µsec.

Actel envisages that designers will use the chips for functions such as level shifting, general-purpose-I/O expansion, address- and data-bus multiplexing and decoding, interface translations, and general glue logic. The 30,000-system-gate part has a static power consumption of 5 µW. Allowing for the I/O orientation of the Plus series, this consumption is as much as 16 times lower power per I/O than that of some competitive devices, the company asserts. The latest release of Actel's Libero-design package includes a pushbutton power-optimization option, which you use as a postdesign step to reduce power usage. It will have a minimal effect on performance, impacting speed by a few percentage points at most. Moreover, the tool gives you feedback on which areas of the design use the most power; a cycle-accurate analysis looks at peak power per cycle as well as average power over the entire simulation. You can also translate this information into a battery-life prediction. Igloo Plus chips will cost slightly less than $2 to $4 (250,000).

> Actel's Flash Freeze feature allows you to place the device in a very-low-power standby mode that nevertheless holds I/O states.

—by Graham Prophet

▷**Actel**, www.actel.com.

MOTOR-DRIVE MICROCONTROLLER HAS TWIN INVERTER OUTPUTS

05.29.08

Renesas designed the SH7137F microcontroller family to meet the needs of designers working on 1- to 100-kW industrial inverters and motor drives. The chip has 256 kbytes of Renesas' MONOS (metal-oxide-nitride-oxide-silicon) flash memory onboard. According to Terukazu Watanabe, chief engineer at the company's microcontroller-business unit, MONOS provides high reliability and access time as low as 10 nsec. It allows devices to run directly from flash memory, removing any need for a cache and saving power.

The microcontroller's 12.5-nsec MONOS supports fully deterministic 80-MHz, zero-wait-state operation. It has two timer units and two 12-bit, fast ADCs for measuring the phase currents. It thus provides for three sample-and-hold circuits in each ADC. The conversion time is as fast as 1.25 µsec. For deeply embedded real-time systems, the device has fast, vectored interrupts; Renesas based it on the SH2 core with 16 32-bit-wide general-purpose registers and a MAC (multiply/accumulate unit) for DSP algorithms. The device comes with a suite of peripherals and I/O ports and is available in 80- and 100-pin QFPs.

—by Graham Prophet

▶Renesas, www.renesas.com.

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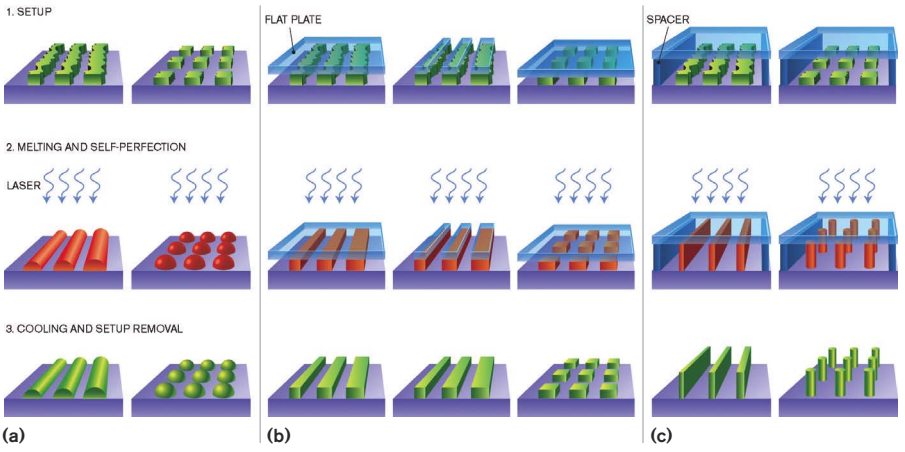

Researchers used open (a), capped (b), and guided techniques (c) for reducing variations and defects.

RESEARCH UPDATE

BY RON WILSON

Melting reduces edge roughness, defects in IC features

A project at Princeton University shows that surface heating of small features on an IC can reduce edge roughness and, in some situations, repair defects in metal and semiconductor structures. Project leader Stephen Chou, the Joseph Elgin professor of engineering at the university, used a pulsed excimer laser to melt surface patterns on a test surface without significantly heating the underlying material—vital in IC processes that must adhere to tight thermal budgets or risk damage to underlying structures such as delicate low-k-dielectric materials.

Chou heated the features for just long enough to melt them—less than a microsecond. When the laser energy stopped, the structures cooled and reformed under the influence of surface tension. Lines became smoother, irregular polygons became more oval or circular, and so on. Perhaps more important, Chou found that he could influence the shape of the material as it cooled by applying a thin quartz flat on the surface of the features. This technique led to flat tops and vertical walls on the resolidified features. In measurements on 70-nm-wide chromium lines, this technique reduced an unspecified measure of edge roughness by a factor of five.

In a further experiment, Chou tried positioning the quartz flat slightly above the melted features. He found that, as the features cooled, they tended to stretch up and grow thinner until the top of the molten liquid touched the plate. The approach resulted in lines that were not only smoother, but also taller and thinner than the original pattern—with obvious implications for increasing control over critical dimensions in some kinds of patterns.

Chou emphasizes that the importance of the technique lies in the fact that, in principle, it allows manufacturers to apply the quartz-plate and laser-pulse process to an entire wafer simultaneously, reducing edge roughness and eliminating small defects for an entire layer of metal or polysilicon features at once. Chou now intends to continue his work by applying the process to 8-in. wafers rather than smaller test areas.

▷**Princeton University**, www.princeton.edu.

05.29.08

NOVEL TRANSISTOR ARCHITECTURES BOOST POLYSILICON SUBSTRATES, THICK-OXIDE GATES

Two research projects into novel transistor structures at the Advanced Technology Institute at the University of Surrey have extended the range of processes that might be able to produce high-performance transistors. Both projects focused on producing high switching speeds and high ratios of on-to-off current in transistors fabricated in "disordered" silicon films–presumably including polysilicon and amorphous silicon. The area is important for at least two reasons: High-performance monolithic transistors on a polysilicon film would open the possibility of fast active devices fabricated directly on solar cells or display panels. And it's much easier to deposit, for example, amorphous silicon on a flexible organic substrate than it is to grow a polysilicon or monocrystalline layer on such heat-sensitive materials.

In the first work, the Surrey researchers demonstrated that a transistor fabricated in a disordered film but with a thin channel–on the order of 2 nm thick–could show on-to-off-current ratios on the order of 10^{11} and very steep subthreshold slopes. In the second project, researchers demonstrated positive switching characteristics in another new structure, the source-gated transistor. These devices have short source-to-drain separation and relatively thick gate oxide. (See, for example, www.guo.ece.ufl.edu/Report6935/Hong.ppt#262,1,Source-gated Transistor.) Work by Surrey professor John Shannon indicated that such devices–which other researchers are exploring for their ability to deal with short-channel effects as semiconductor scaling reaches extremes–also show promise with amorphous-silicon films.

▶**University of Surrey, Advanced Technology Institute, www.ati.surrey.ac.uk.**

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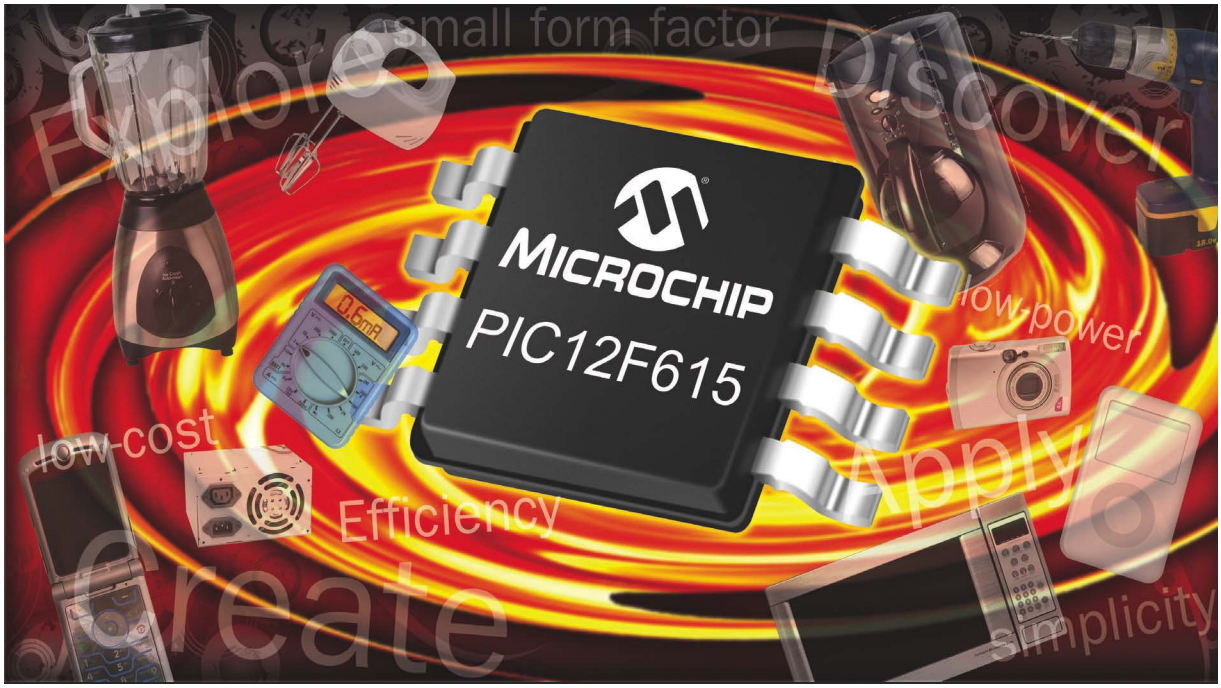

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PIC16F610*	1.75K (1K)	64	12	—	2	1-16 bit, 1-8 bit, 1-WDT	14 pin PDIP, SOIC, TSSOP, QFN
PIC16F616*	3.5K (2K)	128	12	8	2	1-16 bit, 2-8 bit, 1-WDT	14 pin PDIP, SOIC, TSSOP, QFN

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BY HOWARD JOHNSON, PhD

Pointy tips

Some high-speed oscilloscope probes come with tips so pointy and sharp that you can set them down onto a PCB (printed-circuit-board) trace just as gently as a phonograph needle and still pick up a great signal. The sharper the point, the less pressure you need to penetrate the thin oxide layer that coats every copper or solder surface.

I recently obtained a set of such probes. After a while, I noticed the probes working less and less well. They seemed to take increasing amounts of pressure to maintain contact. Soon, I found myself attaching weights to the probes or aggressively taping them to maintain that vital contact pressure. I assumed that the probe tips had just become dull.

To check that assumption, I put the tips under a powerful inspection microscope and saw, to my great amusement, that the tips were not at all dull but simply bent like little elf shoes at the tips. My probes were bent so badly that I was touching the trace with what amounts to the side of the probe tip instead of its end.

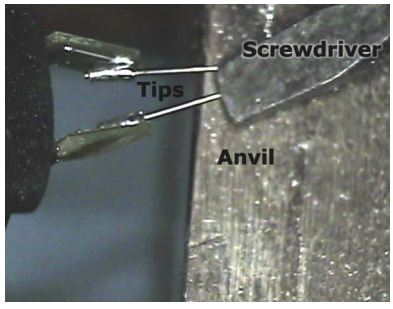
My probes were bent so badly that I was touching the trace with what amounts to the side of the probe tip instead of its end.

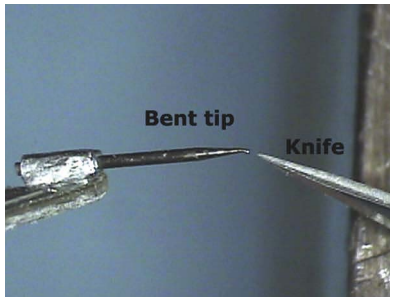
Now, I check my probes frequently. To do that all you need is a 20× power lens—or a 10× lens and really good eyes. When I find a tip starting to go, like this one, I get out two things: a tiny anvil and a hardened-steel screwdriver. For the anvil, I use a drill-press vise. That instrument resembles a miniature bench vise. It is rather flat so that it can hold small things under the spinning chuck of a drill press. Pick one up in a pawn shop or flea market. Mine has hardened faces. You are going to be straightening a couple of hardened-steel pins, so you need tough equipment to do the job.

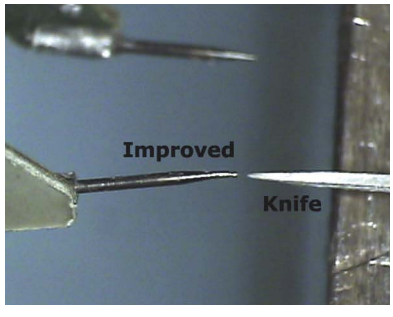
My screwdriver has a high-quality, hardened blade. Many of the pocket-sized screwdrivers for computer work are too soft for this job. Get a real machinist's quality tool. Mine has a blade width of 0.125 in.

Place the probe tip on the anvil and gently stroke it with the screwdriver blade. Watch carefully as you do this. Keep turning the probe so you can see it from all directions so that you know which way to hold it for the next stroke. Just go for a little adjustment at a time; don't break it. After a few passes, the tip will look much better. Keep working, and you can make it look almost brand-new.

Now that I've learned about probe tips, I'm more careful setting them down. Before I touch a trace, I check to make sure that I've completely scraped away the solder mask, and I dress the underlying copper with a little #600 sandpaper glued to the end of a stick. That process thins the oxide, so the probe needs less pressure. EDN







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Go to www.edn.com/080529hj to post a comment on this column and to see a brief video clip on how to straighten probe tips.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Honest energy, part two: Readers respond

Reader response to the last installment of Analog Domain (**Reference 1**) has been both strong and informative—so much so that I'd like to share some of the feedback with you. One reader asks whether home and business owners can borrow compensation schemes that industrial sites exploit, specifically, compensation capacitors for inductive loads. This kind of apparatus works well in industrial applications because the loads are essentially large, fixed, and predictable. Still, the industrial-plant operator must bear the cost of the switching apparatus and of the capacitor bank to abide by standard terms that utilities impose on such customers.

Home and nonindustrial business owners rarely present large inductive loads to the grid. The primary inductive loads in typical households include subhorsepower fuel and circulating pumps for heating systems; compressor motors for refrigerators; and drive motors for dishwashers, washing machines, and clothes driers. All of these comparatively modest loads exhibit small duty cycles, which reduces the benefit of compensating them with expensive apparatus.

Nonetheless, millions of these appliances exist, and the aggregate load is hardly negligible. An economic-compensation scheme that some modern motion-control ICs provide is *electronic* PFC (power-factor correction) as part of their front-end power-management capability. These devices are finding their ways into some of the most energy-efficient air conditioners, washing machines, and other home appliances on the market.

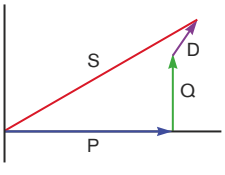

Figure 1 The grid-load, S, is the vector sum of real, reactive, and harmonic power terms, P, Q, and D, respectively.

Another reader correctly points out that I had neglected to mention harmonic distortion in load currents—a term modern grid-current measurements include. In this more complete model, the grid-load vector, S, is the sum of three other terms: the real power, P; the reactive power, Q; and the distortion factor, D (**Figure 1**). The D vector does not lie parallel to either axis because a time-domain transform of the frequency-domain data reveals both in-phase and quadrature components with respect to the real power vector.

Though a negligible concern decades ago, the harmonic content of mains-load current has grown due to the growing prevalence of electronic systems and, in particular, switch-mode supplies. The European Union has led the world in establishing limits on the harmonic content of load currents through standards such as EN 61000-3-2, which defines four load-device classes and the limits on their load-current spectra extending to the 39th harmonic. The influence of this standard extends beyond Europe: OEMs find it economic to ship standards-compliant products worldwide rather than maintain different designs and inventory for different geographic regions.

A third reader suggests that I had not made sufficiently clear in text what the table revealed: Though a typical CFL's (compact fluorescent lamp's) power factor is a disappointing 0.56, on a per-lumen basis, the lamp still improves on a tungsten-filament bulb's grid use by slightly more than a factor of two. Some electronic ballast chips for office-type fluorescent fixtures include PFC, but I've not yet seen the function in CFLs. Let me know whether you do.

This same reader notes a California Energy Commission report that EPRI Solutions and the Lawrence Berkeley National Laboratory prepared (**Reference 2**). I found good introductions to EN 61000-3-2 and -4-13 available from Reo UK Ltd (**references 3** and **4**).EDN

ACKNOWLEDGMENTS

The author thanks readers Jay Salsburg, Mike Patnode, Rich Bingham, M Simon, John Wendler, Tim Hughes, Pen Jennings, and Nick Jancewicz for their feedback and insights. He regrets that space does not allow even brief discussion of all the questions and related topics they raised.

Joshua Israelsohn is a co-founder of JAS Technical Media, where he manages technical-communication services. You can find his contact information at www.jas-technicalmedia.com/contact.

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For a list of references in this column, go to the Web version at www.edn.com/080529ji.

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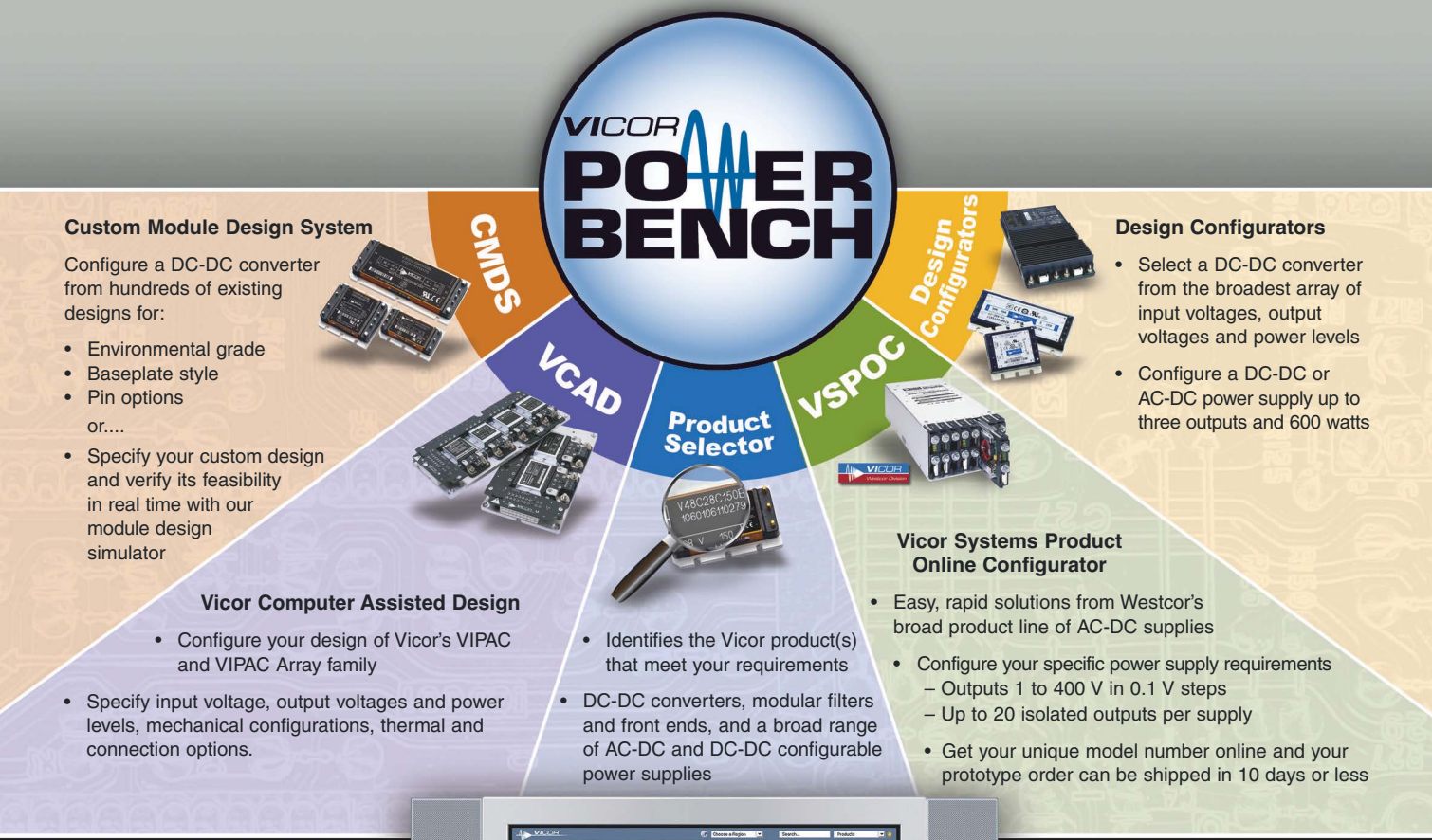

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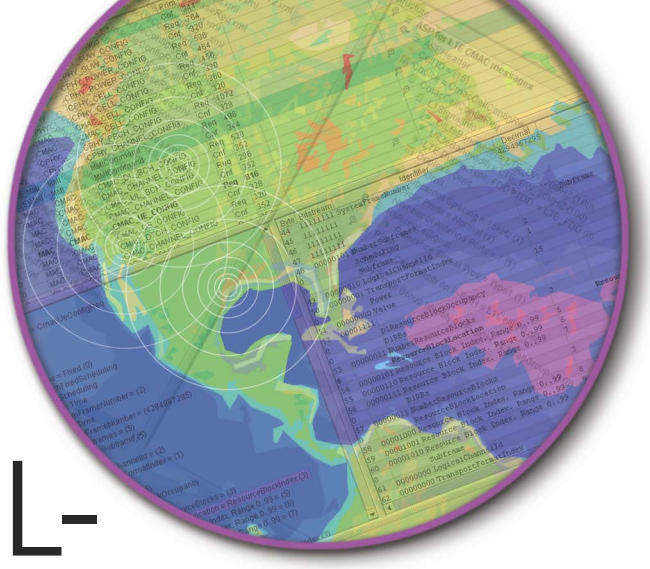

EFFECTIVE TEST STRATEGIES CAN HELP TRANSFORM UMTS INTO A CELLULAR-WIDEBAND SYSTEM.

PROTOCOL-STACK TESTING FOR LTE TECHNOLOGY

BY CHRISTINA GESSNER • ROHDE & SCHWARZ

Producers of mobile phones and mobile infrastructure are working on the next big step in the development of the UMTS (universal mobile-telecommunications system): UMTS LTE (long-term evolution). The new standard will ensure that UMTS remains competitive and give users enhanced mobile-Internet access. The first commercial LTE networks could be in place by 2010, and LTE standardization is progressing as part of Release 8 from the 3GPP (Third Generation Partnership Project). Manufacturers, therefore, will soon need suitable test capability to verify their LTE products.

LTE networks must provide downlink data rates higher than 100 Mbps and uplink rates higher than 50 Mbps. They must also significantly reduce the latency times for packet transmissions so users won't experience unacceptable delays. To achieve these goals, the 3GPP is defining new air-interface-transmission methods and is revamping the protocol and network architecture of UMTS.

Whereas UMTS used WCDMA (wideband-code-division multiple access) for transmitting signals, the LTE downlink uses OFDMA (orthogonal-frequency-division multiple access), which is particularly robust when handling the varying propagation conditions in mobile radios. The LTE uplink will employ SC-FDMA (single-carrier frequency-division multiple access), which is a precoded OFDMA.

Another significant feature of LTE is bandwidth as high as 20 MHz. Because the usable bandwidth is scalable, LTE can also operate in the 5-MHz UMTS-frequency bands or in even smaller bands. Developers of LTE base stations and wireless devices must also account for a transmission-time interval of only 1 msec between data packets.

LTE systems can also employ MIMO (multiple-input/multiple-output) antenna systems. In one MIMO technique, multiple antennas can transmit the same data stream to improve data-transmission reliability, resulting in diversity gain. In another, the antennas use spatial multiplexing—simultaneously transmitting different data streams to increase throughput; this method results in multiplexing gain. Spatial multiplexing is necessary to achieve the greater-than-100-Mbps data rates in the downlink direction.

An LTE base station can have as many as four transmitting antennas, and an LTE wireless device will have as many as four receiving antennas. Initial implementations will probably consist of 2×2-antenna systems—that is, two on the transmitting end and two on the receiving end.

PROTOCOL ARCHITECTURE LTE

The 3GPP is completely reworking the network and protocol architecture of UMTS so LTE can support high data rates and short latencies. LTE is a purely packet-oriented technology whose developers designed it in accordance with the 3GPP's SAE (system-architecture-evolution) effort. LTE uses a minimal network architecture to reduce latency time (**Figure 1**). The LTE base station, or eNB (eNodeB), initiates connections on the air interface. It also assigns air-interface resources and performs scheduling.

Each LTE base station connects to the

core network through the 3GPP-defined S1 interface. The base stations themselves interconnect through the X2 interface so they can initiate and complete actions, such as handovers. As a result, the RNC (radio-network controller) that UMTS used is now unnecessary, which significantly reduces the number of internal interfaces in the network. The eNB basically assumes the functions that the RNC previously handled.

Figure 2 shows the protocol architecture for the user and control planes. The Layer 1 and Layer 2 protocols of the air interface terminate in the wireless device and in the eNB. The Layer 2 protocols include the MAC (medium-access-control) protocol, the RLC (radio-link-control) protocol, and the PDCP (packet-data-convergence protocol). The Layer 3 RRC (radio-resource-control) protocol also terminates in both the wireless device and the base station. The protocols of the NAS (nonaccess stratum) in the control plane terminate in the wireless device and in the mobility-management entity of the core network.

LTE simplifies many of the procedures of UMTS. For example, LTE employs the shared-channel principle, which provides multiple users with dynamic access to the air interface. In contrast to the conventional circuit-switched operation, the packet-oriented LTE network does not assign resources to a user for the entire duration of a connection. Instead, the base station gives the user a resource on the shared channel only when a data packet is ready for transmission. During transmission pauses, LTE can assign the resource to other subscribers. The dedicated channels used in GSM (global-system-for-mobile communication) and UMTS are thus no longer necessary, greatly simplifying the LTE-protocol architecture and ensuring efficient use of the resources on the air interface.

The addition of procedures for link adaptation further improves the performance of the shared channels. With link adaptation, the base station selects the optimum modulation and coding scheme based on the connection quality. The base station also makes frequency-dependent scheduling decisions, such as whether a user would have better connection quality in a specific range of bandwidths. The scheduling mechanism is therefore complex and, if improperly implanted, can significantly degrade the performance of the LTE system. The stringent timing requirements are important because the base station makes a scheduling decision every millisecond.

LTE differs from UMTS in dispensing with the compressed mode of WCDMA, which allows a wireless device to take measurements on other frequencies or radio technologies to optimize call quality and to facilitate handovers. For this purpose, data transmission is compressed so that the wireless device can find gaps for performing measurements. This method is relatively complex to implement. Because LTE doesn't use compressed WCDMA, the base station is responsible for providing subscribers with the necessary pauses for these measurements.

An important aspect, particularly from the point of view of network operators, is the integration of LTE into established mobile-radio networks. In addition to GSM/GPRS (general packet-radio service) and the UMTS networks, these include networks employing WiMax (worldwide interoperability for microwave access) and CDMA 2000. To ensure the successful handover of calls from LTE networks to those based on other technologies, the 3GPP specifies suitable handover mechanisms.

AT A GLANCE

- Manufacturers will soon need suitable test capability to verify their LTE (long-term-evolution) products.
- LTE has bandwidth as high as 20 MHz and can also operate in the 5-MHz UMTS (universal-mobile-telecommunications-system)-frequency bands and even narrower bands.
- During pauses in transmission, LTE can assign the resource to other subscribers, thus obviating the need for dedicated channels, simplifying the architecture, and ensuring efficient use of the resources on the air interface.
- When testing LTE devices, engineers should use a flexible programming language, such as C++, so that they can develop complex test scenarios.

PROTOCOL TESTS

During the early stages of development of LTE-capable chip sets and wireless devices, engineers should perform a

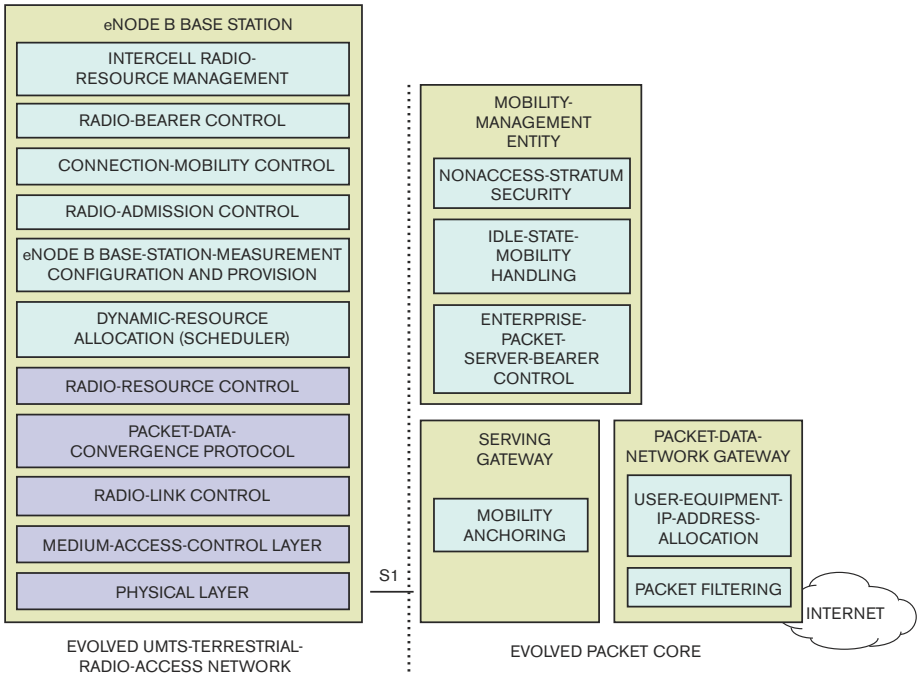

Figure 1 In an LTE network, a base station connects to a core network through the S1 interface. Multiple base stations connect to each other through the X2 interface (not shown).

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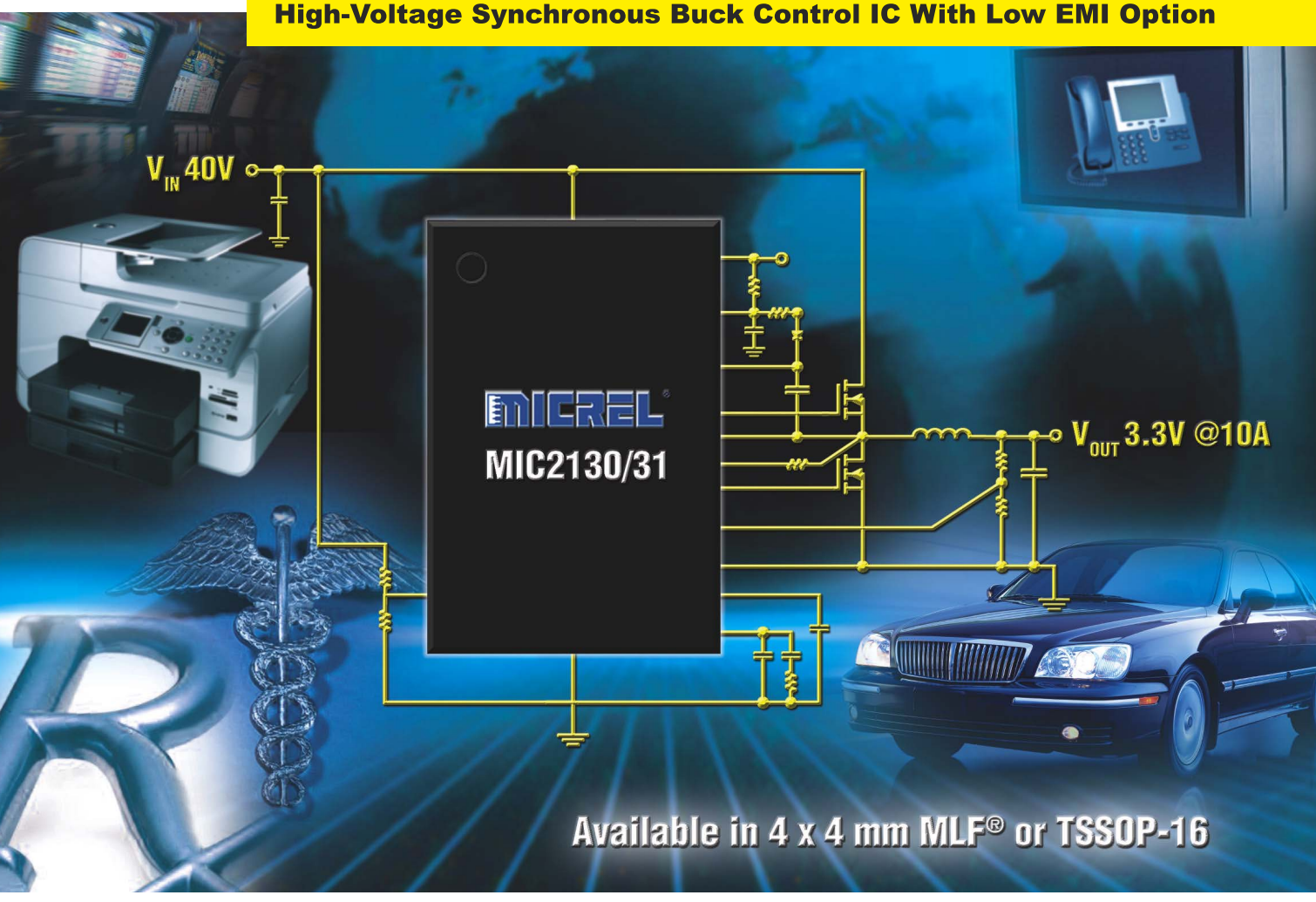

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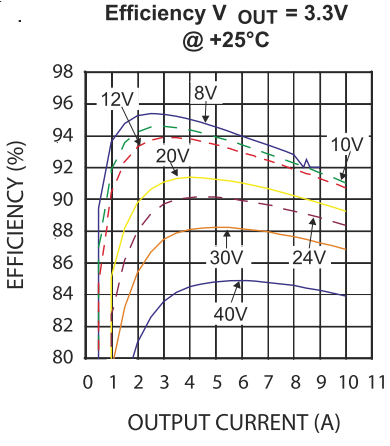

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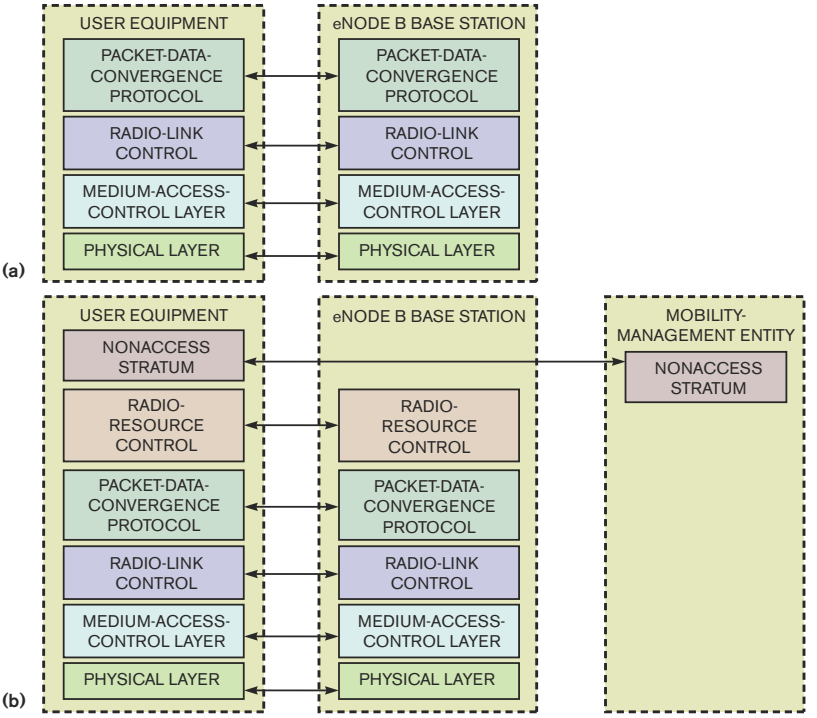

Figure 2 In the LTE-protocol architecture for the user plane (a) and control plane (b), layer 1 and 2 air-interface protocols terminate in the wireless device and in the eNode B base station. The Layer 2 protocols include the MAC protocol, the RLC protocol, and the PDCP. The Layer 3 RRC protocol also terminates in both the wireless device and the base station. The protocols of the nonaccess stratum in the control plane terminate in the wireless device and in the mobility-management entity of the core network.

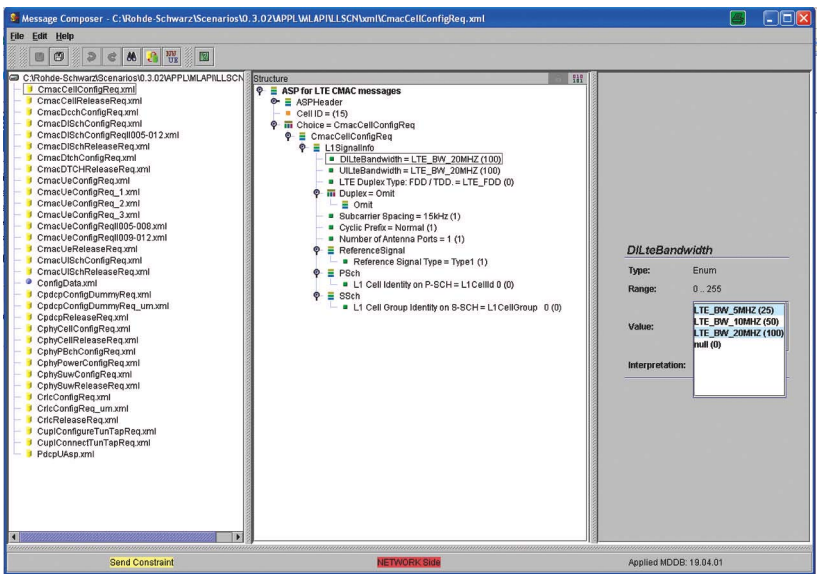

Figure 3 A message composer can help you specify the contents of Layer 3 messages that are used in a test scenario. These messages can perform functions such as setting up a connection.

protocol test and a functional test to ensure that the functioning of the protocols on the air interface complies with the 3GPP LTE specifications. Engineers should also test performance aspects, such as whether the product can handle the high-data-rate requirements of LTE.

Depending on the degree of integration, you can use various approaches for performing protocol tests. Several test-

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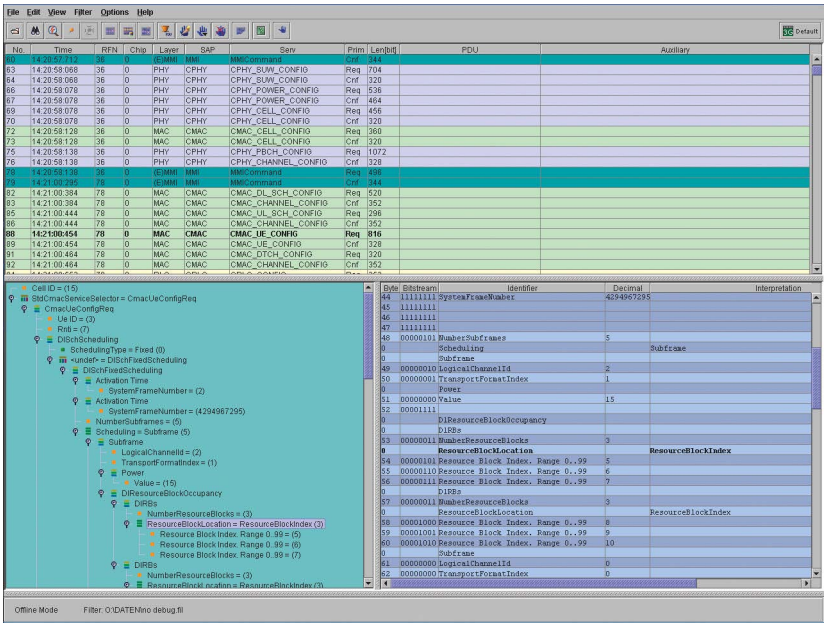


Figure 4 A message analyzer can show every message that the tester and the device under test exchange.

equipment manufacturers offer test instruments that include software-based LTE protocol testers. If a Layer 1 implementation is not yet available or integration has not yet taken place, you can use this software to perform a virtual test of the protocol software. In the Rohde & Schwarz CMW500 for LTE, for example, the test software emulates the behavior of the protocols on the network end. Developers can connect the protocol stack to be tested to a virtual tester using an IP (Internet Protocol) connection. LTE-test scenarios then verify the behavior of the protocol stack on the wireless device end. These scenarios can include a simple connection setup or more complex reconfigurations. You can verify all important functions of the Layer 2 and Layer 3 protocols in the virtual-test environment of the CMW500, for example.

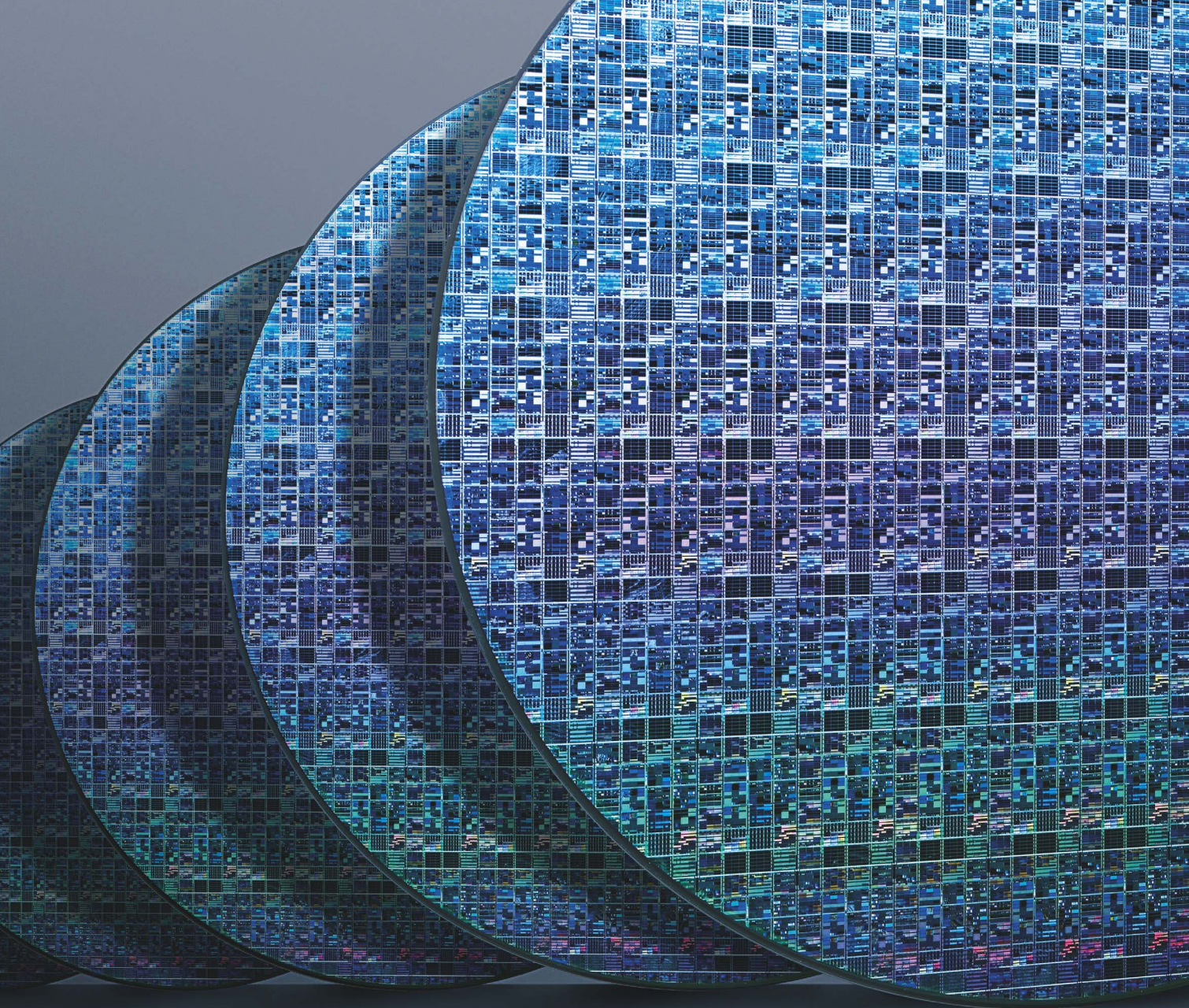
After Layer 1 integration, you can connect the wireless device or chip set to a bench-protocol tester for further testing. The connection can take place using RF or in the baseband—for example, over a digital in-phase/quadrature interface. You can then subject the device under test to the LTE-test cases to study the behavior of the device and detect possible errors.

When moving to the hardware version of a protocol tester, developers can reuse the scenarios from the virtual-test environment. The CMW500 for LTE also provides test cases that include Layer 1 functions. Of interest are the test cases that require an interaction between the downlink and uplink, such as MIMO or the hybrid ARQ (automatic-repeat-request) protocol. For throughput measurements, connection to the user plane—for example, to a video streaming server—is important because it allows the processing of user data in the protocol-test scenario. LTE devices must be able to work with other technologies, because service providers will not simultaneously roll out LTE services everywhere.

TEST SCENARIOS

When testing LTE devices, engineers should use a flexible programming language, such as C++, so that they can develop numerous complex test scenarios. You must make a distinction between the low-level API (application-programming interface) and the medium-level API, depending on whether the interface accesses on top of Layer 2 or Layer 3. The low-level API offers users flexibility for programming Layer 2 of the network simulator. Plus, the low-level API is available early because it requires no Layer 3 implementation. (The 3GPP is still working on the specification of LTE Layer 3.)

On the other hand, the medium-level



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API is an efficient method because the user need not configure layers 1 and 2 on the tester end; Layer 3 automatically handles that task. The user needs to specify only the desired sequence of the protocol-test scenario and the contents of the Layer 3 messages for setting up the connection, for example. **Figure 3** illustrates the use of the CMW500 for LTE for editing messages. State machines allow you to modularly set up the scenarios, so that you can easily reuse components. **Figure 4**, which the CMW500 message-analyzer function generates, shows every message that a tester and a device under test exchange.

INTEROPERABILITY

Manufacturers will soon test the first LTE-capable wireless devices in networks. To comprehensively prepare for these field trials, producers of chip sets and wireless devices will need to perform interoperability tests to test a wireless device in the lab and prepare for all test cases in the field. As a result, they can detect implementation errors early and avoid surprises. If problems do still occur during the field trial, the testers can reproduce scenarios in the lab by using the protocol tester, and they can then eliminate the implementation error from the chip set or wireless device.

The 3GPP is working on test specifications for LTE. In addition to test cases for RF and radio-resource management, the 3GPP will develop numerous signaling-test cases. These cases will include those for layers 2 and 3, as well as NAS-test cases. The 3GPP will describe these test cases in TTCN-3 (testing and test-control notation, Version 3). The conformance test cases that 3GPP specifies will form the foundation for the certification of wireless devices, ensuring that all wireless devices worldwide comply with the same standards.

LTE involves many technical changes for UMTS. Developers of LTE-capable chip sets and wireless devices must early on perform numerous protocol tests to detect errors in the implementation, thus saving time and money. The interworking between LTE and other radio technologies will be an important task in protocol testing. EDN

AUTHOR'S BIOGRAPHY

Christina Gessner has since 2004 been a technology manager for mobile radios at Rohde & Schwarz (Munich, Germany). Her tasks include the development and marketing of the test-and-measurement-product portfolio for UMTS LTE and HSPA (high-speed packet access). After completing her studies in electrical engineering with emphasis on RF engineering at the University of Hannover (Germany) in 1998, Gessner first worked in the strategic-product management of the mobile-radio-networks division at Siemens in Berlin and Munich.

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BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

X86 MICROPROCESSORS MAY NOT HAVE THE ABSOLUTE LOWEST POWER PER MEGAHERTZ, ABSOLUTE HIGHEST PERFORMANCE PER CLOCK TICK, OR OPTIMUM CODE EFFICIENCY WHEN YOU EVALUATE THEM AGAINST ALL POSSIBLE ALTERNATIVES. BUNDLE UP THE FEATURES, THOUGH, AND THE TOTAL "KIT" OFTEN STACKS UP FAVORABLY VERSUS THE COMPETITION.

KEYSTONE OF YOUR NON-PC DESIGN?

Those of you considering PC building blocks for your non-PC designs would do well to keep in mind, as your counterparts who are veterans of this architecture direction have already learned, that placing your stakes on a PC roll of the dice isn't a sure bet. On the one hand, you'll benefit from the tremendous pace of innovation endemic to the PC business, along with low prices resulting from the hundreds of millions of PCs sold worldwide each year. On the other hand, that same tremendous pace of innovation also translates to a tremendous pace of obsolescence, which can be problematic for systems with production cycles that measure longer than six months!

Assuming that you build enough sourcing flexibility into your design to comprehend supply impermanence, PC-tailored microprocessors can provide a cost-effective means of achieving your system's performance targets. And, with the PC industry's amplified power-consumption focus, battery life, power-supply size, and heat dissipation aren't the concerns they might have previously been, either. Traditional CPU and DSP suppliers haven't stood still in the face of the PC-processor onslaught, however, and their alternative solutions remain optimal in many situations. A solid understanding of the historical trends, current status, and future plans of the primary x86 CPU suppliers will enable you to assess which path to take for your next design (see **sidebar** "Montalv-who?").

INTEL: BACK ON TRACK

Intel exemplifies how substantially a company's fortunes can change in five short years. In the early portion of this decade, Intel based its entire microprocessor product line (laptops to servers), with the exception of the Itanium processor, on the NetBurst microarchitecture (see **sidebar** "Speeds and feeds"). NetBurst had lengthy pipelines—20 stages in the initial 180-nm Willamette variant, extending to as many as 31 stages in the final 90-nm Prescott and 65-nm Cedar Mill iterations. These pipelines performed well when code characteristics paired them with highly predictable multimedia-instruction streams. But the low IPC (instructions-per-clock) attribute inherent in any long-pipeline approach, combined with substantial branch-misprediction penalties, gave NetBurst underwhelming performance on more conventional code. And, in striving to boost clock rates as compensation for long-pipeline penalties, Intel ran into substantial leakage-current problems beginning at the 90-nm process node, which rendered the company's NetBurst products 6.2 GHz short of the initial 10-GHz microarchitecture target. (Even getting to 3.8 GHz proved to be a formidable project.)

Intel's fortunes began trending back upward, beginning in the mobile-computing segment, when, in the spring of 2003, it introduced the first Banias iteration of the Pentium M microarchitecture (**Reference 1**). Fabricated on a 130-nm process, Banias preceded the 90-nm-based Dothan with a larger L2 cache and 65-nm dual-core Yonah with a shared L2 cache (**Reference 2**). Pentium M leveraged and expanded on the execution unit of the Pentium III and coupled it to the Pentium 4 bus interface. As such, it offered more efficient power and instructions than NetBurst on a per-clock basis with conventional code traces. Yonah-generation CPUs, instead of using the Pentium M brand of their predecessors, employed a Core marketing moniker that proved somewhat confusing a short time later, when the company rolled out a suite of 65-nm-process-based Merom, Conroe, and Wolfdale CPUs, respectively spanning laptops to servers, and leveraging the follow-on Core microarchitecture, which the company marketed with the Core 2 promotion brand.

Intel is now shipping the second iteration of its Core microarchitecture, known as Penryn, which it fabricates on a 45-nm-process lithography. Penryn reflects the company's "tick-tock" strategy, a product cadence that involves smaller lithography products, with only minor corresponding feature tweaks (tick), followed roughly one year later by a more substantive architecture revamp on a common process foundation (tock).

As such, the corresponding tock to today's Penryn tick, Nehalem, ramps into production this year, and Intel is publicly demonstrating it in prototype-system form. Nehalem will address several longstanding AMD criticisms, albeit ones that few benchmarking tests to date have shown result in real-life performance shortcomings. Through today's Penryn products, all intercore communication, with the exception of intradie shared-cache-coherency synchronization—whether within a

die, between dice in a multidie monolithic-packaged CPU, or between packaged CPUs—occurs through the same front-side bus that carries data traffic to and from external subsystems. The primary external subsystem is the core-logic chip set, which in today's designs contains the DRAM controller.

MANY CAPABILITIES

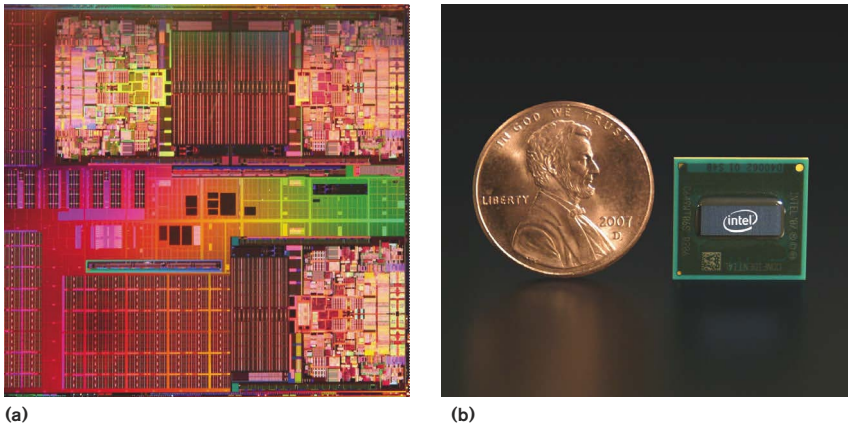
Nehalem-class CPUs integrate the dedicated QuickPath Interconnect interprocessor—formerly, CSI (common-system interface). The link is conceptually reminiscent of the HyperTransport link, which AMD introduced in 2001 for communications between multiple cores on a die and between multiple-die and packaged CPUs. Also reminiscent of technology AMD pioneered in 2003 with the Athlon 64 and Opteron K8 (also known as Hammer) CPUs, Nehalem-based products embed DRAM controllers to, among other things, reduce the extended latencies systems now experience when cache misses require external-memory accesses. And speaking of cache, whereas today's Intel products go beyond two cores by combining multiple die under a common package lid, the prodigious transistor budget that the 45-nm process affords will enable the company to monolithically squeeze at least six CPU cores onto a single sliver of Nehalem-based Dunnington silicon (**Figure 1**). Each pair of cores, like other current products, shares a common L2 cache, and all six cores split a common L3 cache in the layout hole in which a fourth two-core cluster might otherwise go.

AT A GLANCE

- Rapid feature improvements and low prices make x86 CPUs appealing in many non-PC designs.
- After hitting a market-share low point in 2005, Intel has vigorously recovered over the past few years.
- Intel's setbacks boosted AMD's early-decade fortunes; the two companies have subsequently swapped success and failure stories.
- Via Technologies pioneered cost and power concentrations that other x86 suppliers later also embraced. A superscalar out-of-order CPU is finally on the way.

The 45-nm-process generation enables Intel to build not only cost-effective large-die products, but also very cost-effective small-die processors. That cost-effectiveness is the impetus for the Atom-CPU-product line, which Intel formally introduced at the Shanghai Intel Developer Forum in early April (**Reference 3**). Formerly Silverthorne, Atom combines with a single-chip companion device; Intel previously referred to the chip set as Menlow. Atom's origins derive from the under-development and x86-based Larrabee PC coprocessor, intended for graphics, imaging, physics, and other functions. Intel's architects determined that they required the ability to cost-effectively embed 16 or more x86 cores on a single Larrabee die and that the out-of-order execution and other exotic attributes of the company's mainstream CPUs represented overkill for the targeted applications. Consequently, Intel went "back to the future," dusting off its Pentium III schematics to come up with an area-optimized CPU-core design for Larrabee. The company is attempting to maximize its return on investment by also developing few-physical-core chips that it bases on the Larrabee atomic building block, some also with HyperThreading virtual-multicore support, for power- and cost-sensitive mobile systems.

First-generation Atom CPUs come in five versions, with clock speeds that reach 1.86 GHz and a TDP (thermal-design-power) range of 0.65 to 2.4W. Corresponding average- and idle-power ranges are, respectively, 160 to 220 mW and 80 to 100 mW. The partner system-controller hub, available in three versions, features a 3-D graphics core; a hardware-accelerated, high-definition-video-decoding engine; high-definition-audio processing; and support for PCI (peripheral-component-interconnect) Express, USB, and SDIO (secure-digital-input/output) connectivity. And, with long-life-cycle embedded-system designs in mind, Intel promises at least seven years of product support. A planned dual-core Atom variant will be more compelling in low-cost laptop and desktop systems, and Intel also plans an even more integrated single-chip, albeit perhaps multidie, Moorestown Atom family for next year. All in all, after years of stumbling, Intel's seemingly back in full stride. Perhaps the biggest question on the company's road map for the remainder of the decade is the degree to which Atom will cannibalize Intel products in a manner that is fiscally unattractive to Intel, instead of broadening the overall x86 market at the expense of competitors, such as ARM, as Intel hopes.



(a) (b)

Figure 1 An advanced 45-nm-process technology enables Intel to both build ultra-high-transistor-count ICs, such as the upcoming six-core-plus-L3-cache Dunnington CPU (a), and ultrasmall chips, such as the first-generation Atom microprocessor (b).

AMD: DESTINATION UNKNOWN

While key competitor Intel struggled through more than the first half of this decade, AMD "made hay," as the saying goes. The company's K7 Athlon microprocessor, which it introduced in 1999, proved to be a more conventional architecture than the NetBurst-based Pentium 4 Intel unveiled one year later and, as such, was highly clock-efficient from both performance and power-consump-

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tion standpoints. Whereas Intel for many years attempted—largely without success, except in ultra-high-end configurations—to propel the 64-bit-system market to its proprietary, revolutionary Itanium processor, AMD chose a more evolutionary path that appended 64-bit instruction support onto the Athlon foundation. The result was 2003's K8-based Athlon 64 and Opteron (**Reference 4**). K8 CPUs provided other key evolutionary enhancements, as well, such as the earlier-mentioned HyperTransport links and integrated system-memory controllers. And AMD was also first to market with multicore x86 CPUs, at least from a monolithic-die standpoint, judging from 2005's multicore Opteron and Athlon 64 X2 introductions.

The last few years have, however, revealed AMD's key weakness: The company is a much smaller x86 player than Intel, both in employee-head-count and market-share metrics, so the success of each project it tackles is comparatively critical. AMD in 2003 began discussing the architectural goals for the K10 microarchitecture, and the company in 2006 unveiled key details of its 65-nm-process-targeted monolithic quad-core Opteron, Barcelona, and Athlon-follow-on, Phenom. AMD ended up delaying Barcelona's introduction until September 2007 and then further postponed full-production shipments until two months ago, after the company fixed an embarrassing L2 cache TLB (translation-look-aside-buffer) flaw it discovered after Barcelona's launch and coincident with the Phenom unveiling.

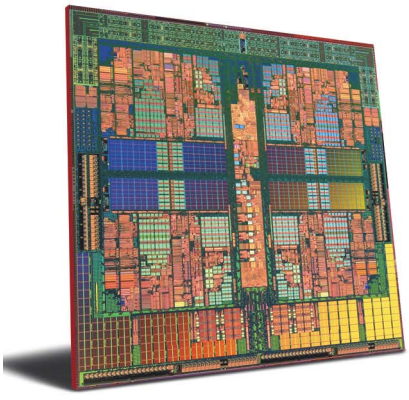

Figure 2 AMD's CPUs' integrated memory controllers and intercore HyperTransport links represent unique capabilities, at least until Intel's Nehalem ramps into production this year.

AMD shipped some Phenom material before the TLB fix, accompanying it with a BIOS-based microcode patch that had the unfortunate side effect of tangibly decreasing performance on many benchmarks. And, in part a reflection of AMD's being one process generation behind Intel, leading-edge Opteron and Phenom CPUs run at core-clock-speed and benchmark deficits compared with their Intel counterparts. On the one hand, this scenario is familiar to AMD; as its mid-1990s P (performance)-rating system suggests, the company's products have long exhibited lower clock speeds but more efficient clock usage than Intel offerings. However, whereas in the early part of this decade AMD was well-matched against Intel's NetBurst-based CPUs, it's now competing against the superior Core-derived follow-ons. AMD's processors' HyperTransport links and integrated DRAM controllers make up some of the clock-speed shortfall, but they can't completely bridge the gap. And, by the time AMD forecasts bringing 45-nm-based K10 follow-ons to market, Intel predicts that it will be ramping its first 32-nm Westmere CPUs into production, thereby preserving its one-generation lithography advantage.

The news, although troubling, isn't all bad on the AMD front. The company's aggressive pricing, at unknown per-product-profit impact, has enabled it to remain largely competitive with Intel in market areas in which its silicon's performance and power-consumption characteristics enable it to have a tangible presence. By virtue of its HyperTransport-based core-interconnect approach, along with other hooks that the K10 design included from the start, AMD can ship some partially defective dice as triple-core Phenom chips, thereby maximizing revenue per wafer (**Figure 2**). AMD is also moving its K8-based dual-core CPUs to the 65-nm process, which should improve their die-per-wafer usage and therefore increase AMD's combination of dedicated and foundry-supplied fabrication capacity.

Like Intel, AMD sells some of its products in embedded flavors with extended-life-cycle guarantees, enhanced testing, and other attributes that non-PC customers value. And AMD also continues

MONTALV-WHO?

In 1995, start-up Transmeta began working on a then-secret chip design. Over time, word leaked out that the company was readying an Intel-targeting, low-power x86 processor for portable-system applications, and, by the time Transmeta formally unveiled its plans in January 2000, public anticipation had reached fever pitch. Transmeta produced two product lines, Crusoe and Efficeon. Although Transmeta is now a shadow of its former self, having jettisoned the bulk of its staff and transformed itself into an IP (intellectual-property)-licensing entity, its industry influence lives on in the power-stingy chips that Intel and its competitors now sell.

Similarly secretive, several-year-old start-up Montalvo Systems may be following in Transmeta's footsteps. Basing opinions solely on tantalizing rumor tidbits and a few filed patents, industry observers believe that the company is readying a low-power-x86-compatible-processor line based on an asymmetrical, function-specific, multicore architecture. To date, the company has raised more than $73 million in private-equity funding, and its staff includes such long-term veterans of the Intel wars as Matt Perry, Transmeta's former and Montalvo's current chief executive officer, and Vinod Dham, the former vice president of Nexgen, former Intel chief architect, and former AMD vice president.

Information at press time suggests that Montalvo is running low on cash and seeking either additional private investment or a buyout. Will Montalvo ever turn its microprocessor vision into silicon, and, if so, will it be successful? There's more than one way to profitably return a backer's financial investment; Transmeta, for example, successfully concluded in late 2007 a 2006 lawsuit against Intel to the tune of $250 million.

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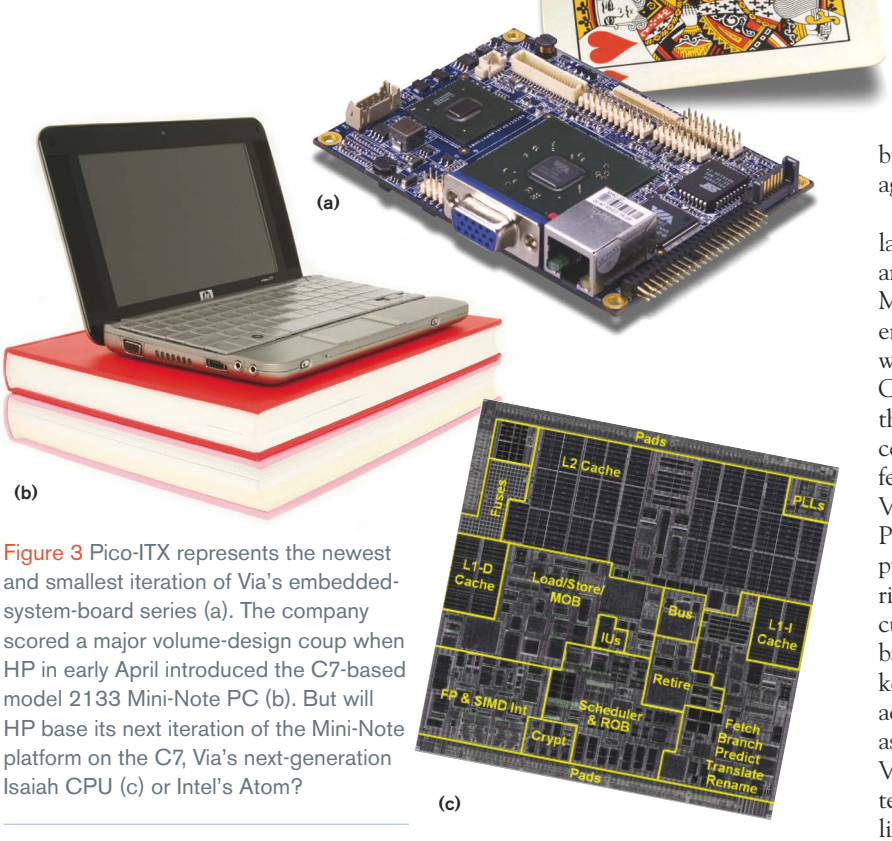

Figure 3 Pico-ITX represents the newest and smallest iteration of Via's embedded-system-board series (a). The company scored a major volume-design coup when HP in early April introduced the C7-based model 2133 Mini-Note PC (b). But will HP base its next iteration of the Mini-Note platform on the C7, Via's next-generation Isaiah CPU (c) or Intel's Atom?

to sell the Geode integrated-x86 line, which it acquired from National Semiconductor in 2003 and whose legacy extends back to the Cyrix MediaGX. (National Semiconductor purchased Cyrix in 1997.) Although AMD doesn't officially comment on future plans for Geode, the most recently unveiled product variant, Geode LX, dates from 2005, and the company shut down its Geode-design center in 2006.

VIA: SCRAPPY UNDERDOG

Via Technologies, long known as a core-logic-chip-set supplier, also became a CPU manufacturer in September 1999, when it acquired IDT's Centaur Technology subsidiary. (Via also purchased National Semiconductor's PC-specific Cyrix assets in September 1999.) From its beginnings, Centaur has consistently focused on minimizing die size and power consumption and striving to deliver sufficient performance for conventional applications. This stance was controversial in the company's early years, when a "clock-rate-is-everything" mentality dominated the industry. However, such thinking has become more mainstream.

The company's series of C3-generation CPUs, known in fanless configurations as Esther, today predominantly derives from the Nehemiah core, though Via bases some C3 products on the older Samuel 2 design (**Reference 5**). Nehemiah features various general-architecture enhancements, such as a full-speed floating-point unit, a deeper pipeline, a more comprehensive MMX (multimedia-extensions) implementation, and a switch from 3DNow! to SSE (streaming-single-instruction/multiple-data-extensions)-enhanced multimedia-instruction sets. Nehemiah also targets embedded-system designs, such as twin thermal-based hardware RNGs (random-number generators). Via refers to these RNGs as PadLock RNGs and, in a later proliferation, an AES (Advanced Encryption Standard) engine, PadLock ACE. Single-chip CoreFusion products combining Nehemiah CPU and north-bridge core-logic die in a unified package are also available.

For more conventional desktop and laptop designs, such as Hewlett-Packard's recently introduced model 2133 Mini-Note PC, along with higher end embedded-system applications with and without fans, Via also offers its C7-class CPUs (**Figure 3**). The company built them on partner IBM's 90-nm SOI (silicon-on-insulator) process, and they offer enhanced PadLock capabilities. As Via's documentation describes, "The Via PadLock Security Engine in the Via C7 processor adds SHA [secure-hash-algorithm]-1 and SHA-256 hashing for secure-message digests, and a hardware-based montgomery multiplier supporting key sizes up to 32 [kbytes] in length to accelerate public-key cryptography, such as RSA [Rivest/Shamir/Adleman]. The Via C7 also provides NX execute protection, providing protection from malicious software, such as worms and viruses, and is used in Microsoft Windows XP with SP2. Integrating security directly onto the processor die ensures speeds and efficiency many times that available in software, yet with negligible impact on processor performance."

Reflecting the company's core-logic heritage, a range of companion chip sets for Via's CPU families provides system-design flexibility, with integrated options such as 2- and 3-D graphics acceleration and hardware-accelerated decoding of MPEG-2, MPEG-4, and other video codecs. External-interface options include single-data-rate SDRAM, double-data-rate SDRAM in multiple generations, parallel- and serial-ATA (advanced-technology-attachment) mass storage, PCI and PCI Express add-in

SPEEDS AND FEEDS

This article contains a large number of processor-project and -product names without providing detailed information on most of them. The omission was intentional for two key reasons. First, available page count is limited, and I've chosen to be comprehensive of vendors, architectures, and product lines rather than the specifics of any product. Second, many of the products in this article are not yet in production, and specifications will inevitably evolve, rendering obsolete some of the data I might include. The good news is that *EDN*'s Web site provides a timely and unlimited supplement to this article. Hit Google, Zibb, or your favorite search engine to peruse EDN.com for already-published write-ups and keep an eye on the *Brian's Brain* blog for article addendums, identifiable by their "Embedded x86" tag lines.

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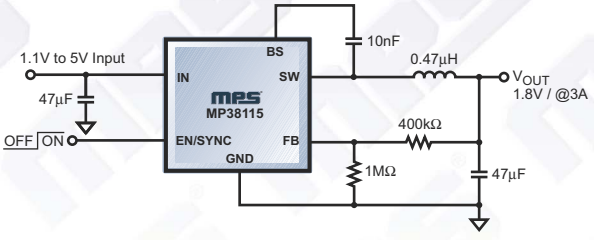

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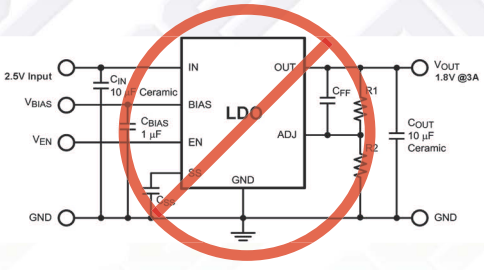

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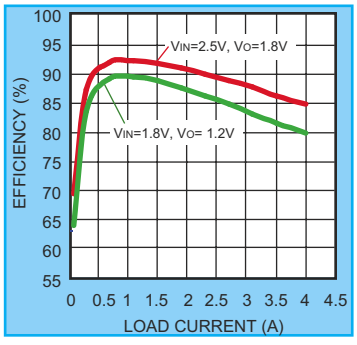

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The 21×21-mm NanoBGA2 package common to many C3 and C7 CPU proliferations efficiently uses available system-board real estate. Speaking of system boards, if you'd prefer not to design your own, Via will happily sell you one of its 6.7×6.7-in. (170×170-mm) mini-ITX, 4.7×4.7-in. (120×120-mm) nano-ITX, and 3.9×2.8-in. (100×72-mm) pico-ITX boards. Effectively shrunken PC motherboards, they come in a diversity of CPU, core-logic chip-set, and support-chip combinations, including 10/100-Mbit Ethernet and GbE (gigabit-Ethernet) transceivers, greater-than-two-channel surround-sound analog and digital audio, TPMs (trusted-platform modules), IEEE-1394-interface ICs, and analog-video encoders, along with DVI (digital-video-interface) and LVDS (low-voltage-differential-signaling) digital-video outputs.

The mini-ITX form factor, which Via unveiled in 2001, is the most mature of the three options, and the company's success in promoting it as an industry standard has attracted competitive attention. Third-party partners sell mini-ITX boards based on both AMD and Intel CPUs, and Intel also manufactures its own mini-ITX products. Notably, the company has shown several Atom-based mini-ITX designs at numerous public forums in recent months.

And speaking of Atom, Via's competitive CPU response, Isaiah, is key to the company's future viability. Ironically, as Intel has stripped out-of-order execution and other superfluous features from its previous architectures, thereby resulting in an approach somewhat reminiscent of Centaur's nearly decade-old vision, Glenn Henry, president of Via's Centaur subsidiary, and his design team are poised to unleash Via's first three-way superscalar out-of-order architecture. The company formally unveiled Isaiah in late January. It also adds support for 64-bit instructions, hardware virtualization, and other much-needed features of modern competitive CPUs. Via will initially fabricate Isaiah on a 65-nm foundry lithography, in which design targets include doubling the integer performance and quadrupling the floating-point performance over that of the Via C7 at equivalent clock speed.

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Isaiah's 65-nm power-consumption target is a 25W TDP at 2 GHz. Via is currently scheduling first Isaiah-based products for production in the second quarter, marking a one-quarter slip from the original publicly stated schedule. The company should be shipping the chips by the time you read this or soon thereafter. Via will provide companion core-logic chip sets for the CPU. And, in an interesting partnership perhaps reflecting the company's shrinking market share in the AMD- and Intel-targeted core-logic markets, Nvidia will sell Isaiah-tailored chip sets, too. EDN

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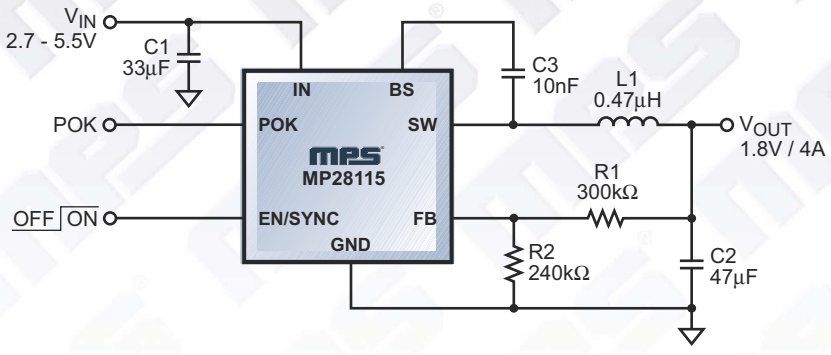

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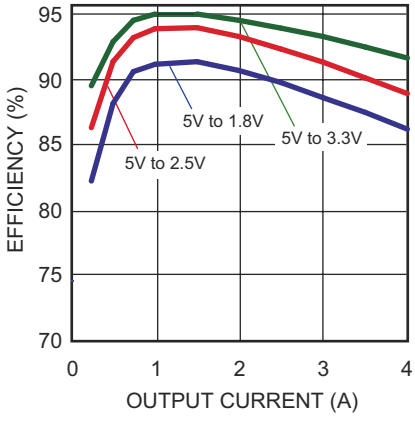

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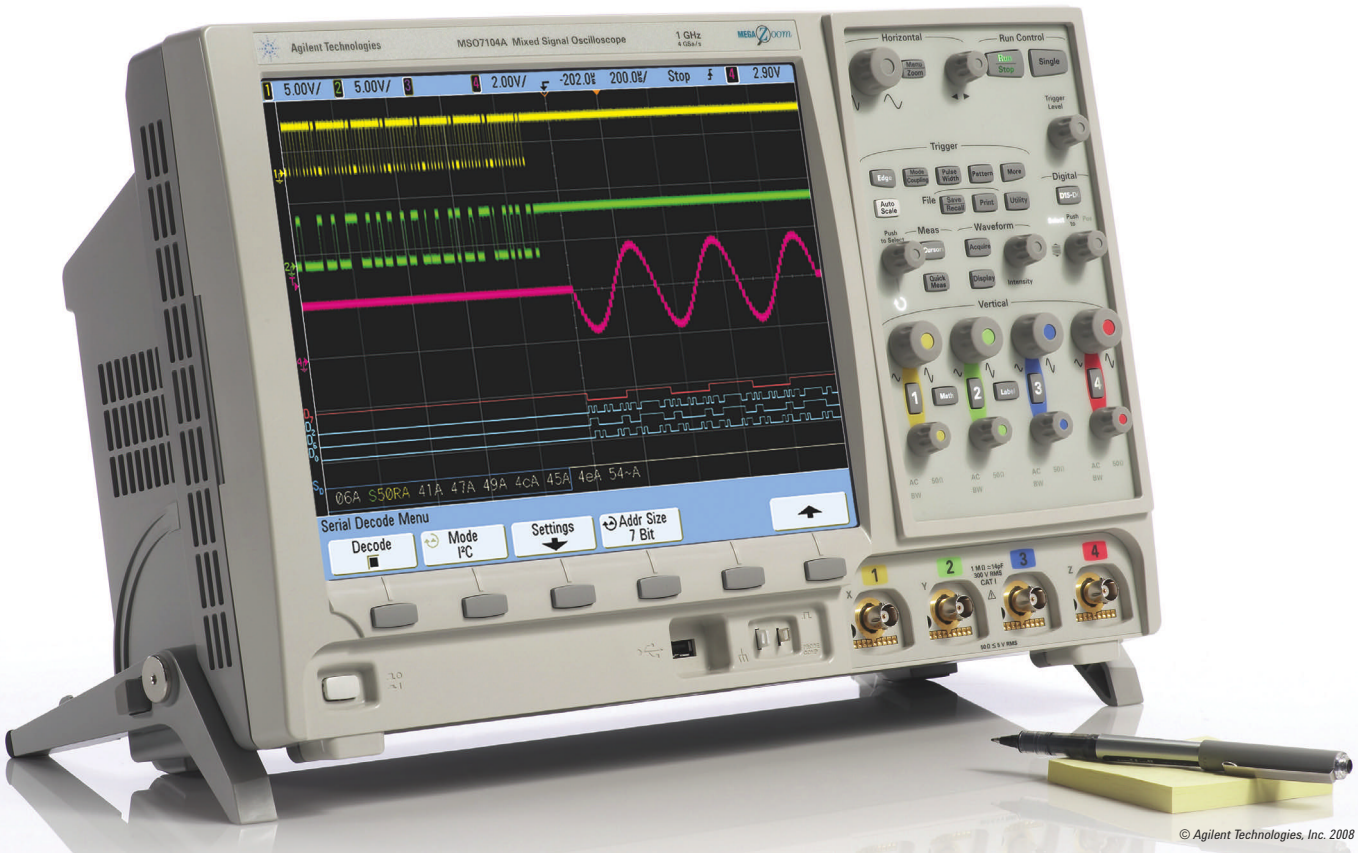

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BY SATISH DHANASEKARAN AND DARRIN RUSSELL • AGILENT TECHNOLOGIES

Unraveling the dynamic-range specification in modern spectrum analyzers

USING A RELATIVELY SIMPLE CHART TO CALCULATE DYNAMIC RANGE, ALONG WITH SPEED AND ACCURACY SPECIFICATIONS, ENSURES THAT YOU CHOOSE THE RIGHT SPECTRUM ANALYZER AND MAKE APPROPRIATE PRICE/PERFORMANCE TRADE-OFFS.

Wireless-communication technologies are evolving from 2G, 2.5G, and 3G to 3.9G technologies. Consumer demand for seamless access to data and personal content—that is, voice, music, and video—is driving this technology evolution. The goal of modern wireless communication is to provide users with faster and more sustainable data rates in more locations. The technologies are also using expensive spectra to provide carriers with cost advantages. To provide the high data rates that some applications require, modern technologies have had to increase the channel bandwidths or use more bandwidth-efficient transmission schemes. According to the Shannon Theorem, channel capacity scales directly with bandwidth. To provide sustainable data rates over the air, designers must implement special mechanisms in protocol for faster link adaptation, higher-order modulation, and channel-coding schemes.

Transceiver-design teams are looking for cost-effective ways to test their designs to pass the technical requirements that the standards impose. In the past decade, the advent of faster and better ADCs and DACs, faster and cheaper DSP technology, and integrated RF (radio-frequency) modules have resulted in increasing the performance specifications of test-and-measurement equipment. This article highlights some approaches designers can take when making the price/performance trade-offs with spectrum analyzers.

Dynamic range—the difference between the highest and the lowest power signals that you can simultaneously measure on a spectrum analyzer—is a key gauge of the instrument's performance. The dynamic range affects the adjacent-channel response, spurious response, and other key regulatory measurements. Dynamic-range performance combines the distortion and noise-floor performance of the spectrum analyzer. It is important to evaluate the dynamic-range performance of the analyzer in the context of the application or the standard in which the analyzer will find use. Understanding the measurement requirement from an application standpoint could potentially save costs in the purchase of test-and-measurement instruments and may improve test margins and productivity.

A combination of air-interface standards and regulatory bodies, such as the Federal Communication Commission, dictates the performance requirement for a generic transmitter (**Figure 1**). The specifications that relate to spectral purity, including spectral emissions, adjacent-channel-power ratio, and alternate-channel-power ratio, are critical for transmitter designers. **Table 1** presents an example of a system-level-transmitter-emission specification. The **table** also attempts to use system-level specification and deduce subsection-level specifications. Some sections of the radio have more stringent specifications

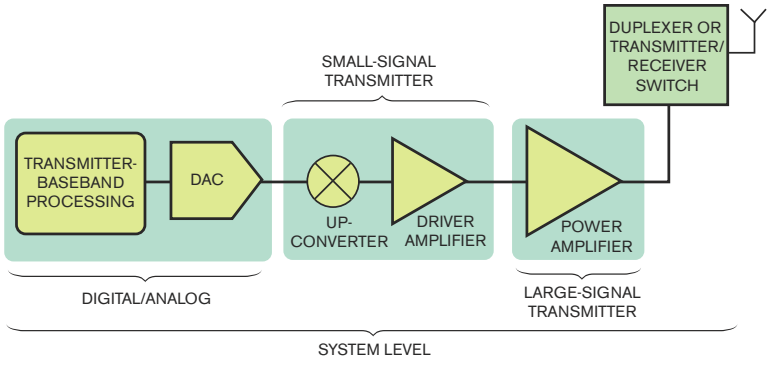


Figure 1 A combination of air-interface standards and regulatory bodies, such as the Federal Communication Commission, dictates the performance requirement for a generic transmitter.

TABLE 1 DYNAMIC-RANGE SPECIFICATIONS

Specification	Standards body/FCC	System level	Power-amplifier level	Transmitting	Digital/ analog
Power level (dBm at 10-MHz bandwidth)	33	33	34	20	−10
7-MHz offset	−58	−58	−61	−68	−71
25-MHz offset	−70	−70	−73	−80	−83

that require better performing instruments to make these measurements. The transmitter signal at the output of the digital/analog module typically has the strictest spectral performance requirements and requires analyzers with the best dynamic-range performance.

Spectrum analyzers target specific price-performance points, and you can classify them as having low, economy, midrange, and high performance. The manufacturer's data sheet provides key specifications to determine whether a spectrum analyzer can meet the measurement requirements. The dynamic-range chart lists these specifications, including displayed-average-noise level, third-order intercept, and second-order-harmonic intercept (**Figure 2**).

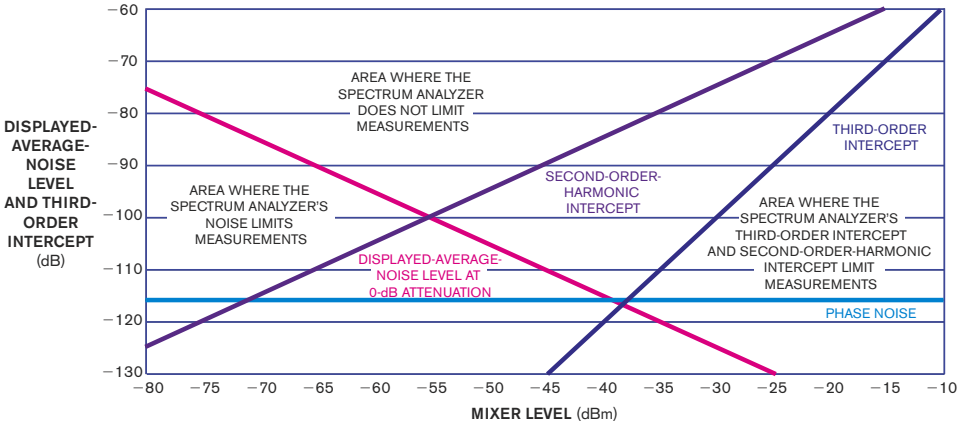


Figure 2 The dynamic-range chart lists these specifications, including displayed-average-noise level, third-order intercept, and second-order-harmonic intercept.

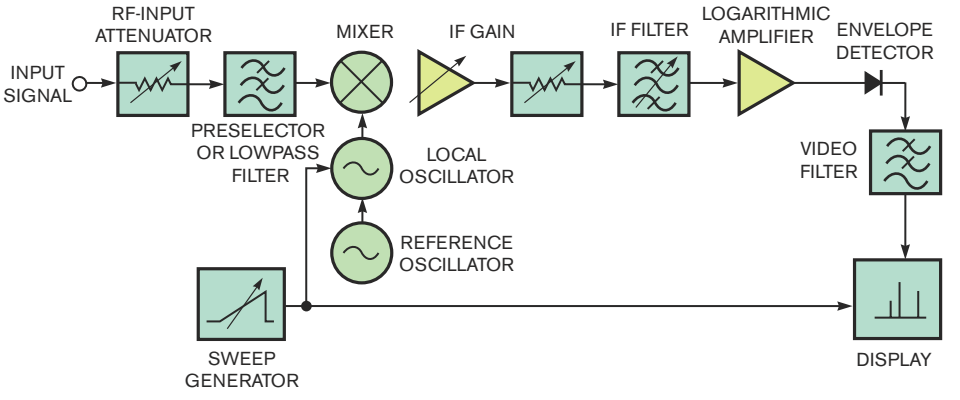


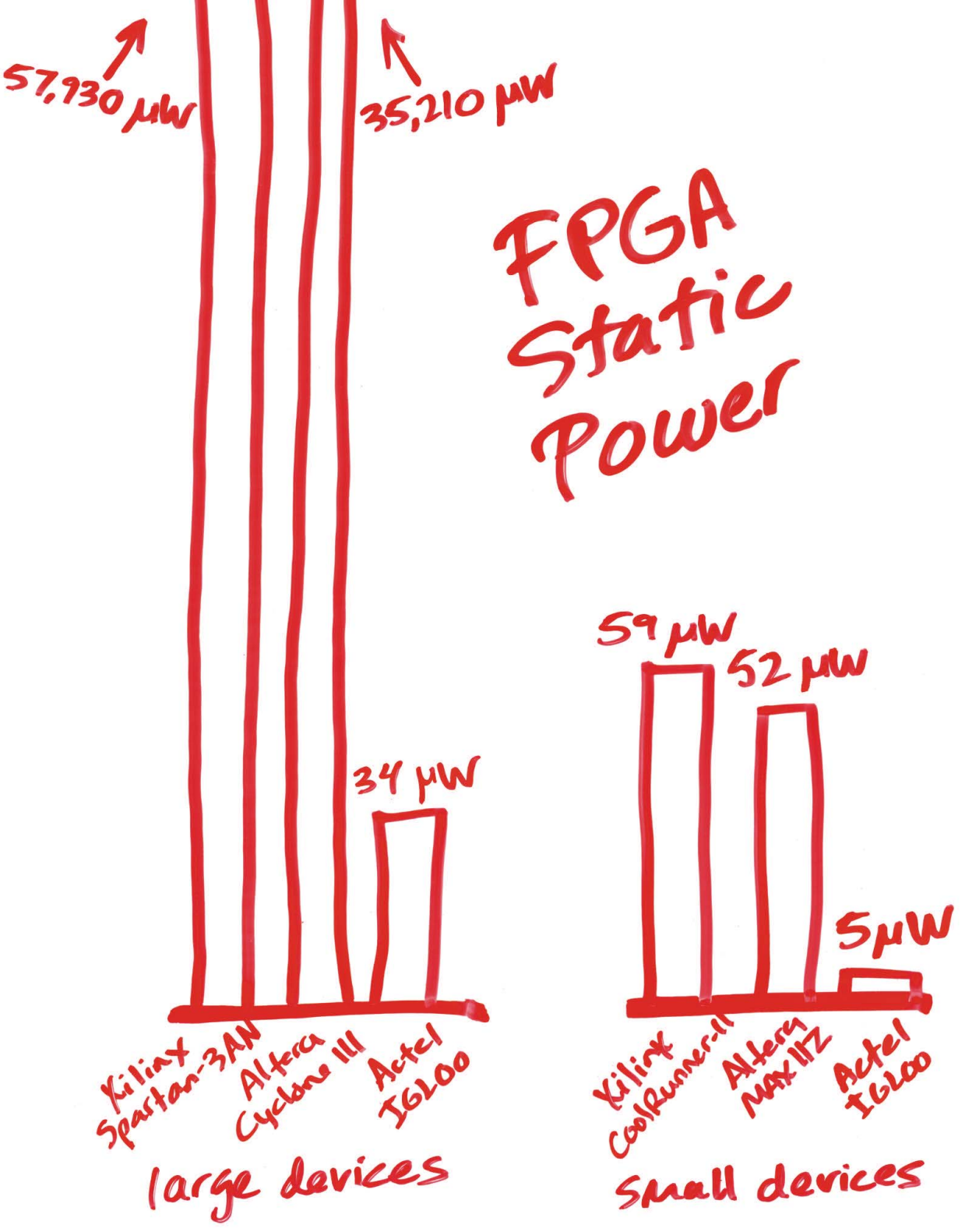
Figure 3 The major factors that help quantify a swept-spectrum analyzer's dynamic range are distortion performance, broadband-noise floor, and local-oscillator phase noise.

DYNAMIC RANGE

The major factors that help quantify a swept-spectrum analyzer's dynamic range are distortion performance, broadband-noise floor, and the phase noise of the local oscillator (**Figure 3**). The distortion performance includes third-order intercept and second-order-harmonic intercept. The front-end mixer in the analyzer typically dominates this specification. Broadband-noise floor refers to the sensitivity floor of the analyzer. This article takes a closer look at how each one of the above factors affects the spectrum analyzer's dynamic range. A complete discussion on how the spectrum analyzer works is beyond the scope of this article; however, **references 1** through **3** provide more detail.

The input section of the analyzer has an RF attenuator; a preselector or a lowpass filter; a mixer, which downconverts the RF to IF (intermediate frequency); and an IF amplifier whose gain couples with the input attenuator. The mixer's second-harmonic distortion and third-order intercept determine the analyzer's distortion performance. The spectrum analyzer's data sheet provides these figures at different measurement frequencies. It also provides a graphical representation for different input levels to the mixer. The mixer input level in decibels referred to milliwatts is the difference between the input signal you apply to the analyzer and the RF-input-attenuation level. For measurements at RF and microwave frequencies, the third-order intermodulation products fall inside the band of interest and thus dominate most spectral measurements. The third-order-distortion products follow the $2\times F_1-F_2$ and $2\times F_2-F_1$ rule (**Figure 4**). You can generally ignore the second-order products when the measurement bandwidth is less than twice the fundamental frequency. In general, the odd-order products fall at close proximity to the measurement frequency, and the even-order products fall at multiples away from the frequencies of interest. Typically, the third- and fifth-order intermodulation products of active components such as mixers and amplifiers tend to dominate the ACPR (adjacent-channel-power-ratio) measurements. RF designers must measure the true distortion performance of the device under test. For the ACPR measurement to reflect the true performance of the device under test, the distortion within the analyzer must be significantly lower. As a point of reference, if the distortion performance of the analyzer is 18 dB lower than the device under test, measurement uncertainty will be less than 1 dB (**Reference 4**).

By reducing the input-signal level to the analyzer's mixer, you reduce the levels of the third-order-distortion products by a factor of two. You can achieve lower levels to the mixer by increasing the analyzer's input-attenuation level. However, increasing the attenuation directly affects the noise floor, reducing the dynamic range. Therefore, the optimal attenuator setting becomes a trade-off between third-order intercept and noise-floor performance. Although two-tone analysis may



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seem too simplistic for most digital-communication formats, it can serve as a useful starting point because you can use a summation of tones to represent wide-bandwidth signals (**Figure 5**). When you look at them in this way, you can easily see that the third-order-intermodulation products are within one main-channel bandwidth away from the carrier—that is, in the adjacent channel. Likewise, the fifth-order products fall within two main-channel bandwidths away—that is, in the alternate channel. With this simplified view, it is immediately obvious that, at different offsets from the main channel, different factors affect the measurement.

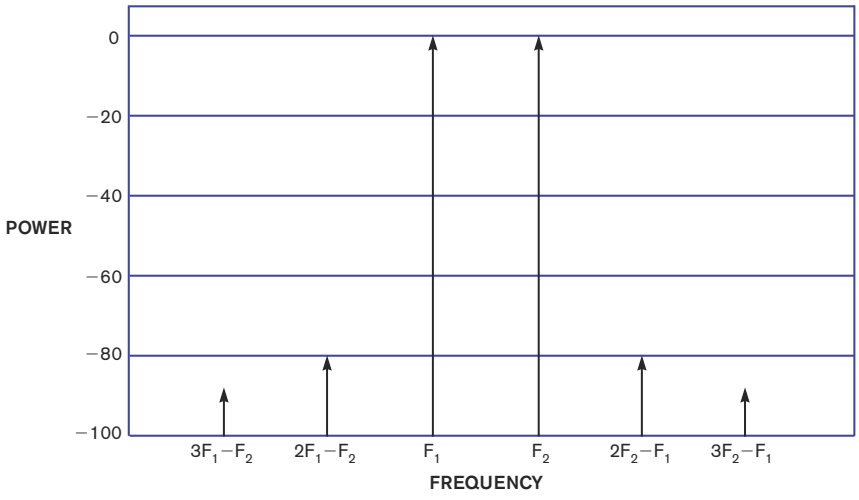

Figure 4 For measurements at RF and microwave frequencies, the third-order-intermodulation products fall inside the band of interest and thus dominate most spectral measurements. The third-order-distortion products follow the $2\times F_1-F_2$ and $2\times F_2-F_1$ rule.

The spectrum analyzer's data sheet specifies displayed-average-noise level, which is a measure of the ultimate sensitivity of the spectrum analyzer. Manufacturers typically specify this figure with 0-dB input attenuation and normalized to a 1-Hz resolution bandwidth. The noise floor of the analyzer increases decibel for decibel as the input attenuation increases. As you increase the resolution bandwidth of the filter, the noise floor of the analyzer increases to 10 times the logarithm of the ratio of the resolution-bandwidth increase, and the sweep time decreases, speeding the measurement. This mechanism allows engineers to trade off dynamic-range performance for measurement time. Using the dynamic-range chart helps you determine the optimal mixer-input and attenuation levels. The

intersection of third-order intercept and noise-floor sweep provides the optimal mixer-input level for maximizing dynamic range. This optimized mixer-input level provides a trade-off between noise floor and distortion performance (**Figure 6**).

To further improve the dynamic-range performance, some spectrum analyzers apply averaging and trace-math calculations to subtract the analyzer-generated noise from the measurement. In practice, noise correction can provide as much as 10-dB improvement in noise-floor performance. Noise correction has two main benefits. One is the ability to subtract the noise contribution of the analyzer from a noise-limited measurement. The second is to allow the user to apply additional attenuation to decrease the internal third-order intercept of the analyzer without increasing the noise floor for third-order-intercept-limited measurements.

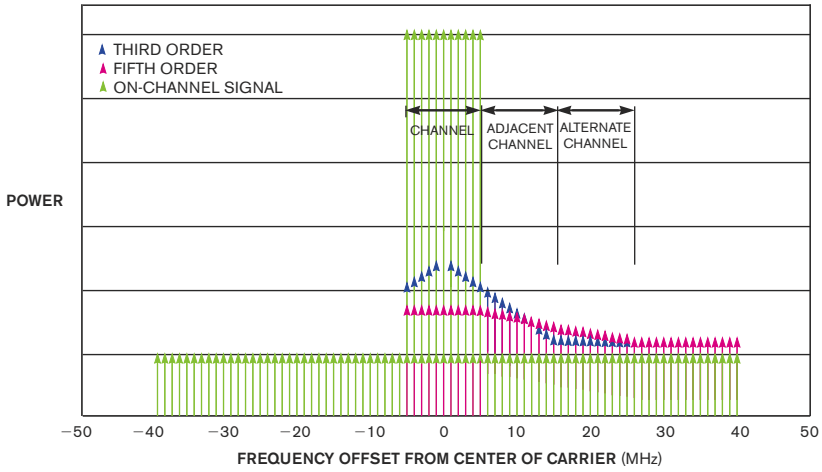

Figure 5 Although two-tone analysis may seem too simplistic for most digital-communication formats, it can serve as a useful starting point because you can use a summation of tones to represent wide-bandwidth signals.

PROBLEMS WITH PHASE NOISE

The phase noise of the local oscillator in the analyzer can also degrade an analyzer's noise-floor performance at offsets close to the carrier. In general, at offsets greater than 1 MHz, the phase noise does not impact the dynamic-range performance. The following example provides more details. Consider a digitally modulated signal with a channel bandwidth of 10 MHz. The intent is to measure the spectral emissions at an offset of 5.1 MHz

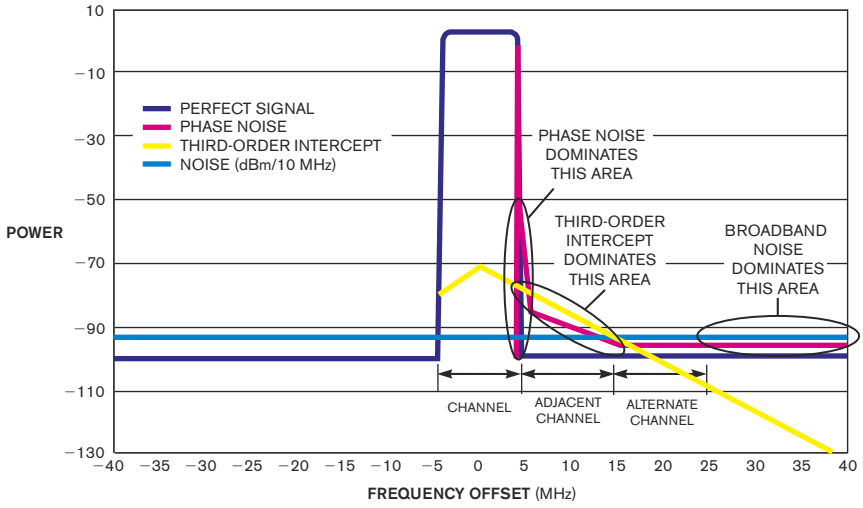

Figure 6 The intersection of third-order intercept and noise-floor sweep provides the optimal mixer-input level for maximizing dynamic range. This optimized mixer-input level provides a trade-off between noise floor and distortion performance.

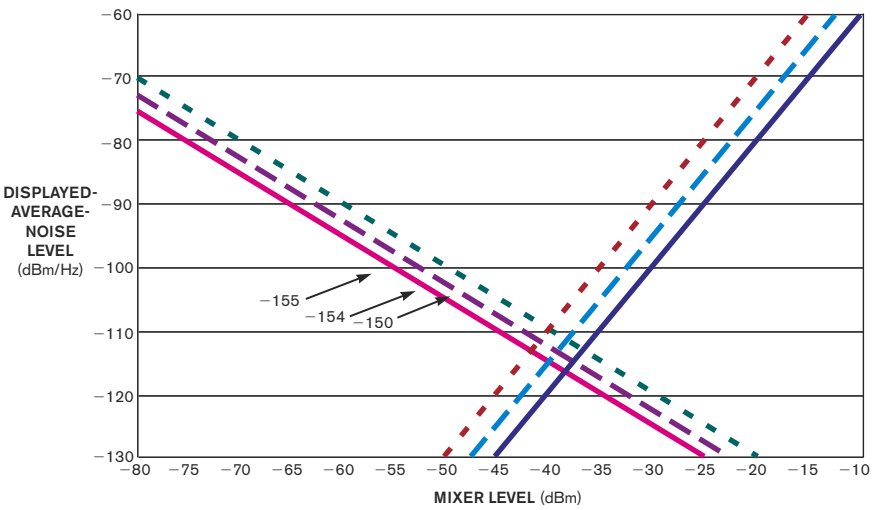

Figure 7 By combining the dynamic-range charts of various analyzers, you can deduce each device's performance limitations.

from the center frequency in a 100-kHz integration bandwidth. The transmitter power is −20 dBm. If you assume that the analyzer's third-order intercept is 19 dBm, the third-order-distortion product is −78 dBc at an integration bandwidth of 10 MHz or −98 dBc at an integration bandwidth of 100 kHz. The 5.1-MHz offset represents a 100-kHz offset from the edge of the main channel. Assume that the data sheet documents the phase noise of the analyzer at 100 kHz to be −115 dBc/Hz. The total noise in the 100-kHz bandwidth is then −115 dBc+50 dB=−65 dBc/100 kHz. For close-in offsets, the analyzer has a 65-dB dynamic range. At offsets more than 1 MHz away, the phase noise of the analyzer improves and does not represent a limitation for dynamic range.

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You can apply the basic understanding of the dynamic-range chart to the measurement requirements for the transmitter system in **Figure 2** and **Table 1**. You must use external at-

tenuators to protect the spectrum analyzer if the power from the device under test is above the maximum power level that the analyzer specifies. The goal of this exercise is to present customers with the ability to select the spectrum analyzer that meets their measurement needs.

By combining the dynamic-range charts of various analyzers, you can deduce each device's performance limitations (**Figure 7**). Remember that the most stringent requirements are on the digital/analog module. So, a high-performance analyzer would be the best fit for this application. It is important for customers to also look at other specifications, including maximum frequency range, error-vector-magnitude floor, amplitude flatness, and analysis bandwidth, before deciding which spectrum analyzer to purchase. **EDN**

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AUTHORS' BIOGRAPHIES

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Multicore-programming frameworks for embedded-multimedia applications

UNDERSTANDING THE DATA-ACCESS PATTERN OF AN APPLICATION CAN HELP YOU EFFECTIVELY USE THE MEMORY AND SYSTEM RESOURCES OF THE UNDERLYING ARCHITECTURE TO DEVELOP A SCALABLE PARALLEL APPLICATION.

It is becoming difficult to meet the growing processing demands of embedded-multimedia applications with single-core architectures. Although multicore embedded architectures have emerged as a promising solution to this problem, they bring with them the challenge of developing software that efficiently uses them. Current compiler technology and development tools require more sophistication to make multicore architectures successful. You develop most parallel software by converting sequential programs to parallel programs by hand, and a lack of multicore-aware developmental tools makes the software difficult to evaluate. Without solid project planning up-front, you may be facing inefficient applications and an increased time to market.

Software frameworks can provide a better starting point for developing multicore applications and thus help to reduce the development time. This article demonstrates frameworks for embedded-multimedia applications; however, you can extend the data-flow models to many other applications. The frameworks incorporate the inherent data parallelism in multimedia applications and demonstrate effective management of streaming data by efficiently using the underlying architecture.

There are two significant challenges to producing parallel software in which you can scale the performance of a sequential application to the number of available cores: developing efficient parallel algorithms and efficiently using the shared resources such as the memory, DMA (direct-memory-access) channels, and interconnect network.

There are often several ways to parallelize an application. Some applications exhibit inherent parallelism; others have extremely complex and irregular data-access patterns. In general, scientific applications and multimedia applications are often easier to parallelize, because their data-access patterns are more predictable than those of control applications. This article discusses parallelization techniques targeting multimedia algorithms, which require high processing power and are attractive for embedded-system applications.

Levels of data parallelism exist in multimedia applications. The granularity of parallelism varies greatly from a set of frames to a macroblock of a frame. In general, the lower the granularity, the higher the level of synchronization you need between the sharing elements—cores and DMA channels, for example. Lower granularities increase parallelism and reduce network traffic; higher granularities require lower synchronization but also increase the network traffic. So, based on the application type and system requirements, the frameworks define different levels of parallelism.

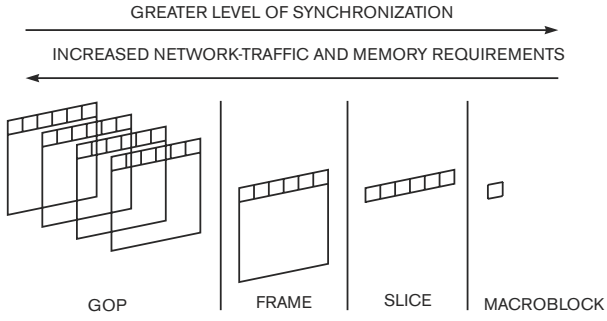

Figure 1 Multimedia applications exhibit various levels of data parallelism that result in corresponding trade-offs.

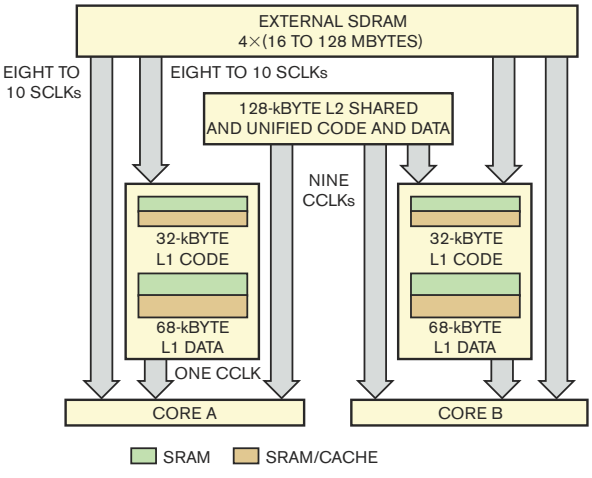

Figure 2 The ADSP-BF561 architecture consists of separate instruction and data memory private to the two cores and a shared L2 and external memory.

As noted, developing scalable parallel software also depends on the efficient use of the interconnect network, memory hierarchy, and the peripheral/DMA resources. The strict low-power and low-cost requirements of a system constrain all of these elements. Efficient use of these resources when programming in a multicore environment requires innovation. This article presents some ideas to help efficiently manage these resources on Analog Devices' Blackfin ADSP-BF561 dual-core processor.

MULTIMEDIA-DATA-FLOW ANALYSIS

To achieve data parallelism, the goal is to find a block of data or a set of blocks of data in the streaming data that you can treat independently and "feed" to a processing element. Independent blocks of data reduce synchronization overhead and make parallelizing algorithms easier. To find this data, it is important to understand the data-flow model, or the "data-access pattern," of an application.

For most multimedia applications, you can view the data-access pattern as a 2-D pattern (spatial domain), in which the independent blocks of data are confined to a single frame, and a 3-D pattern (temporal domain), in which the independent blocks of data span more than one frame. In the spatial domain, you can divide the frame into slices with N sequential rows and macroblocks of a video frame. In the temporal domain, you can subdivide the data flow at a frame level or a GOP (group-of-pictures) level.

Algorithms with a slice or macroblock data-access pattern require greater synchronization but have less network traffic, as the memory hierarchy needs to store only a part of the image data. In the case of a frame- or a GOP-type data-access pattern, the memory hierarchy needs to store large amounts of data but requires considerably less synchronization, as the system exhibits higher granularities of parallelism. **Figure 1** shows levels of parallelism that exist in a multimedia application; it correspondingly shows the relative synchronization and the network traffic between the four levels.

MULTICORE-ARCHITECTURE ANALYSIS

Figure 2 shows the ADSP-BF561 architecture, which consists of separate instruction and data memory private to the two cores and a shared L2 and external memory. You can interface all peripherals and DMA resources to either core with configurable-arbitration schemes. There are two DMA controllers, each of which consists of two sets of MDMA (memory-DMA) channels. A separate bus connects the L2 memory and each core. A shared bus connects the external memory and the two cores.

All of the frameworks use DMA to move the streaming data within the memory hierarchy. The other alternative, cache memory, does not manage any data. You know the data-access pattern for the applications you are targeting; thus, you can effectively use the DMA engine to manage data. The cache suffers from nondeterministic access times, cache-miss penalties, and increased external-memory-bandwidth requirements. Using the DMA engine, you can transfer data to L1 memory before a core request; the system performs transfers in the background without halting the core for a data-item request.

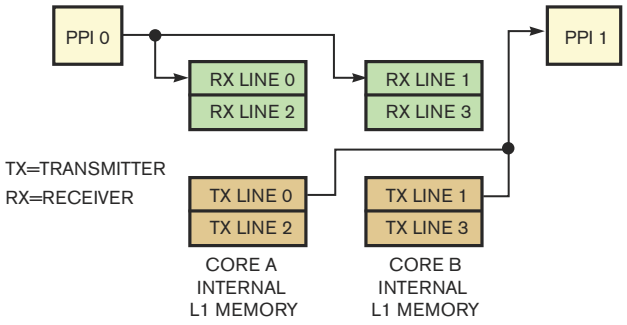

Figure 3 In the line-processing framework, Core A handles the video input, and Core B manages video output.

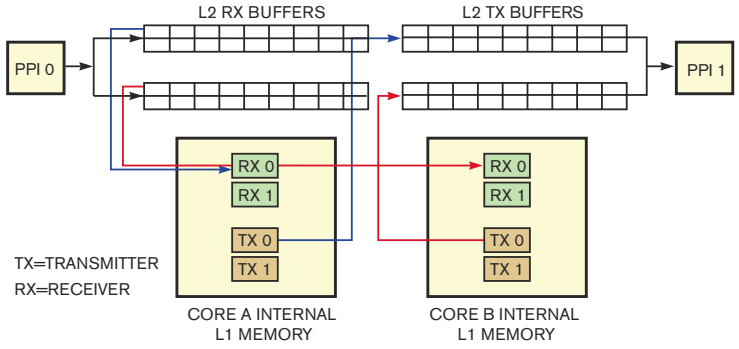

Figure 4 In the dual-core macroblock data-flow model, the L2 memory maintains multiple slice buffers, and separate MDMA channels transfer macroblocks from L2 to L1 memory of each core.

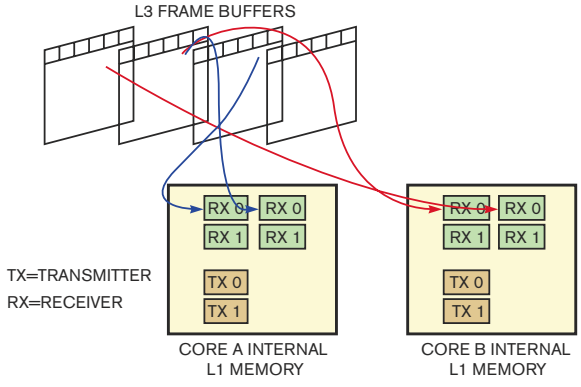

Figure 5 In frame-level processing, external memory stores the dependent frames.

With two sets of MDMA channels on each DMA controller, the system evenly distributes MDMA channels among the cores for symmetrical parallel processing.

You can easily exploit the fast access time of L1 and L2 memories for applications with smaller granularities of data-access patterns. You can directly transfer the independent blocks of data to L1 or L2 memory from the peripheral interface without accessing the slow external memory—saving valuable external-memory bandwidth and MDMA resources and reducing data-transfer time.

For applications in which higher levels of granularity char-

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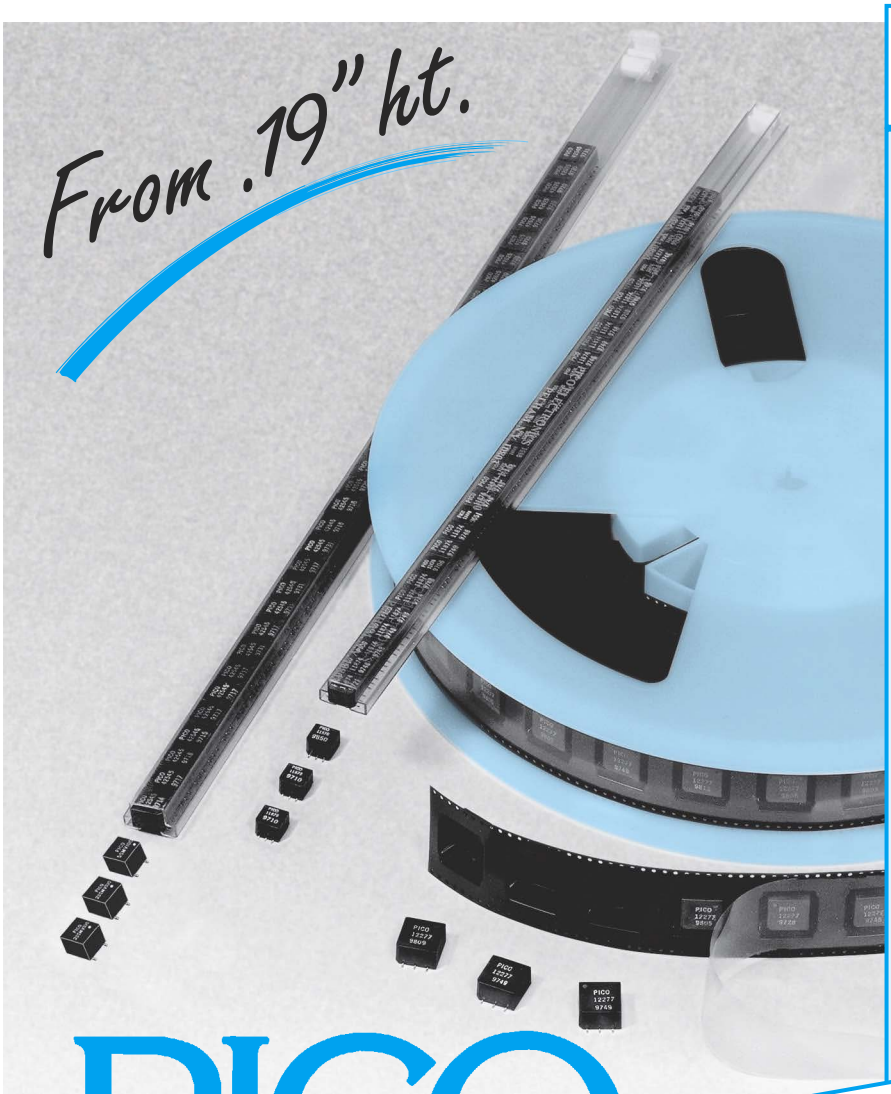

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acterize the data-access pattern, memory becomes a bottleneck, as the smaller L1 and L2 memory levels are insufficient to hold multiple frames of data. However, although the data dependency exists between multiple frames, the dependency is more often than not over only the smaller blocks across frames. If you could store all the dependent frames in a larger memory space (external memory), then you could sequentially transfer only the independent blocks from each frame to the available cores for processing. If these independent blocks of data are considerably smaller than the frame data, so as to fit in the memory space of L1 or L2, you can efficiently process the data with lower memory-access latency.

Two cores share the L2 and external-memory-interface bus, although separate buses connect both memory levels. Thus, you should minimize simultaneous access by the two cores to the same memory level to avoid stalls due to contention. To minimize contention, the frameworks map code and data objects such that only one core maximally accesses the L2 core; the other core maximally accesses external memory. In this case, the core performing most of the external-memory accesses has greater memory-access latency, but overall access latency is less than the cost of contention.

The framework assigns all input-peripheral interfaces to one core and all output-peripheral interfaces to the other core. The frameworks use a video-in/out example using the PPI (parallel peripheral interface) to input and output video frames. The BF561 architecture has two PPIs.

If the interrupt processing time is less than the processing time of the streaming data, you can assign all peripheral interfaces to one core for ease of programming; the lower interrupt processing time will not affect the load balancing between the two cores.

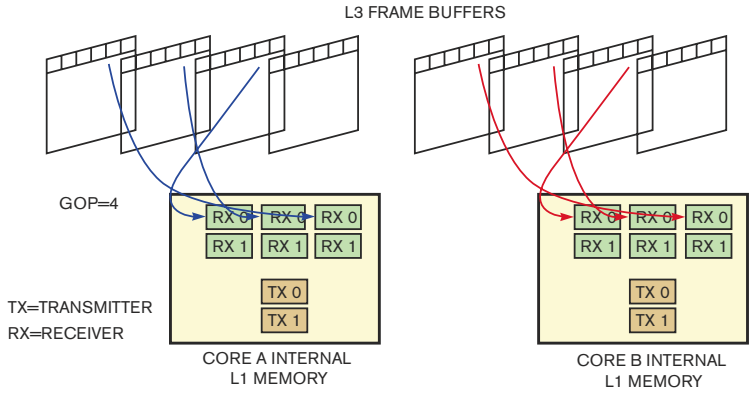

Figure 6 For a GOP-type data-access pattern, dependency exists within a set of frames, and there is no data dependency between two sets of frames.

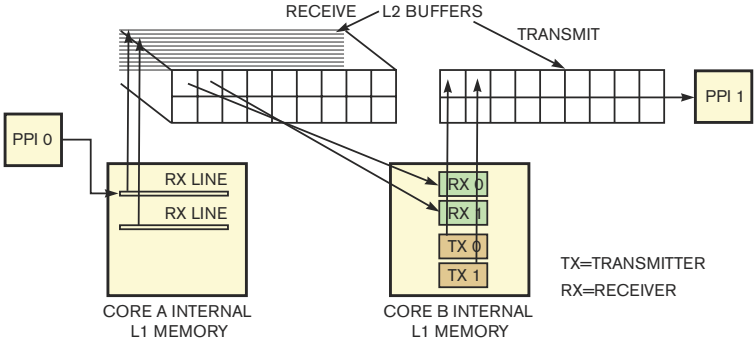

Figure 7 The data flow combines the line- and macroblock-processing frameworks.

PROPOSED FRAMEWORK MODEL

Based on the granularity of the data-access pattern, you can define four frameworks: line processing (spatial), macroblock processing (spatial), frame processing (temporal), and GOP processing (temporal). If the data-access pattern of an application fits one of these four models, you can use the corresponding framework. There are also ways to integrate multiple frameworks for asymmetrical parallel processing when you have two or more processing algorithms for a data stream.

In the case of line processing, dependency exists only at a line level—that is, between adjacent pixels. Every line forms a data block that each core can independently process. **Figure 3** shows the data-flow model for the line-processing framework. Core A handles the video input, and Core B manages video output. Separate sets of MDMA channels manage data between Core A and Core B. L1 memory uses multiple buffers to avoid contention between core and peripheral-DMA access. A counting semaphore ensures that every line achieves synchronization between the two cores. A single-core imple-

TABLE 1 FRAMEWORK SPECIFICATIONS

Template	Core cycles/pixel× approximately single core	Core cycles/pixel× approximately two cores	L1 data memory required (bytes)	L2 data memory required (bytes)	Comments
Line processing	42	80	Line size×2; 1716×2 for ITU-656		Double buffering in L1
Macroblock processing	36	72	Macroblock size N×M×2	Slice of a frame; (macroblock height×line size)×4	Double buffering in L1 and L2
Interframe processing	35	70	Size of subprocessing block×number of dependent blocks	Size of subprocessing block×number of dependent blocks	Only L1 or L2 can be used, double buffering in L1 or L2

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mentation of this framework also takes advantage of moving data directly into the L1 memory, thereby saving external-memory bandwidth and DMA resources. Examples of applications that can use this framework include color conversion, histogram equalization, filtering, and sampling.

Figure 4 shows the data-flow model for the macroblock-data-access pattern. You can move alternate macroblocks between the two cores. The L2 memory maintains multiple slice buffers, and separate MDMA channels transfer macroblocks from L2 to L1 memory of each core. L1 memory also maintains multiple buffers to avoid contention between DMA and core access. Similar to the line-processing framework, Core A handles the input-video interface, and Core B manages the output interface; a counting semaphore achieves synchronization between the two cores. Targeted example applications for this framework include edge detection, JPEG/MPEG-encoding/decoding algorithms, and convolution encoding.

In frame-level processing, external memory stores the dependent frames. Depending on the granularity of dependency between frames (macroblock or line), the system transfers subblocks of frames to the L1 or L2 memory. **Figure 5** shows the data flow for the frame-level-processing framework. In this case, assuming a macroblock dependency across multiple frames, the system transfers macroblocks of frames to the L1 memory. Similar to the other frameworks, Core A handles the input-video interface, and Core B manages the output interface. A counting semaphore achieves synchronization between the two cores. Example applications for this framework include motion-detection algorithms.

In GOP-level processing, each core processes multiple sequential frames. The difference between the frame-processing framework and the GOP-level framework is that the frame-processing one performs spatial division within frames, whereas the GOP-level one uses temporal division (sequence of frames) to implement parallelism. For a GOP-data-access pattern, dependency exists within a set of frames, and there is no data dependency between two sets of frames. Thus, cores can independently process each set. **Figure 6** shows the data flow for this framework. Similar to the frame-processing framework, the system can transfer blocks of frames to the L1 memory of the cores. To efficiently use the interleaved memory-banking structure of the external memory, the system equally divides the banks among the cores. Each external bank of the ADSP-BF561 supports as many as four internal-SDRAM banks. Examples of applications that could use this framework include encoding/decoding algorithms, such as MPEG-2/4.

In a more real-world application, multiple algorithms running within the system process the streaming data, and each of these algorithms may exhibit a different data-access pattern. In such cases, you can combine the frameworks for a particular application. To take advantage of the multiple cores you can pipe-

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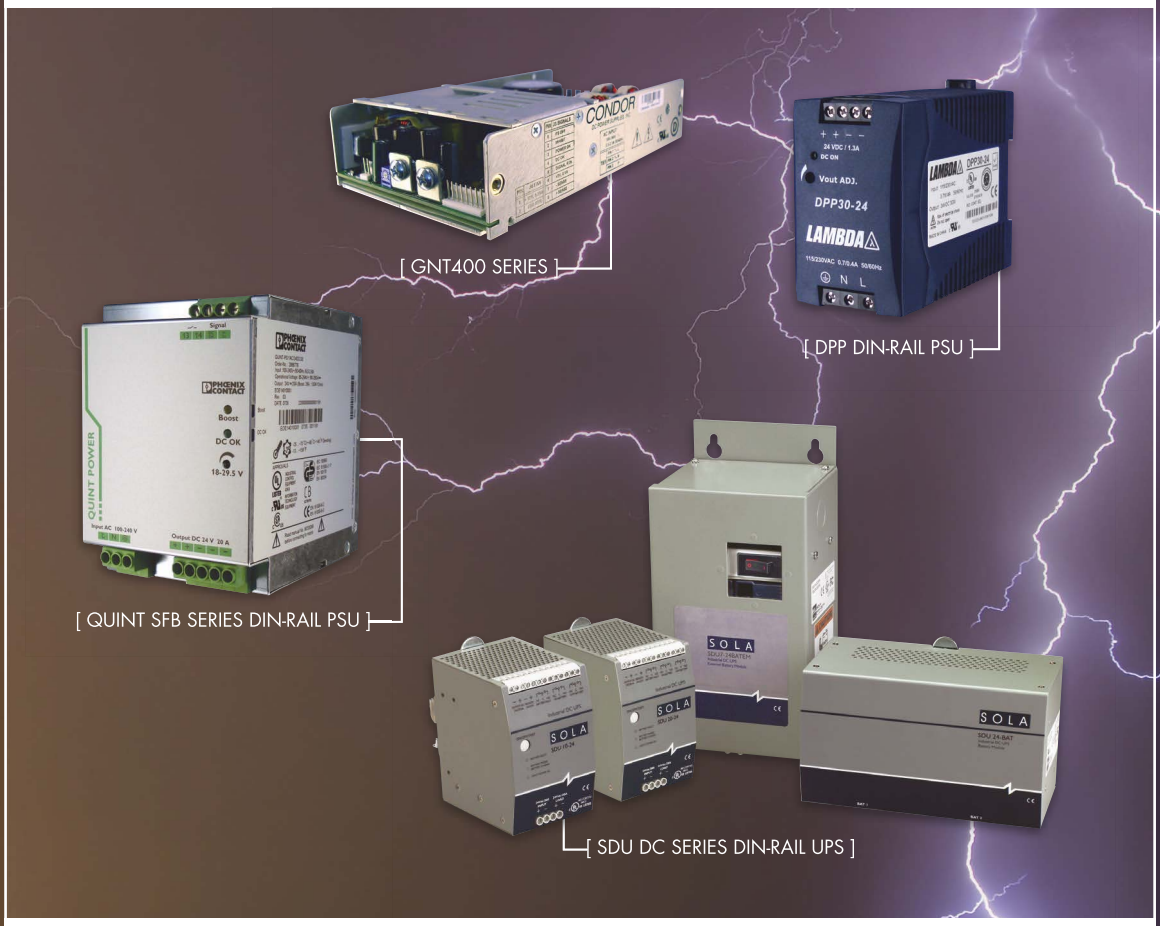

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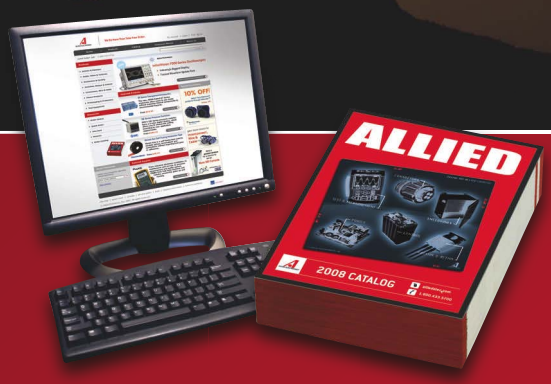

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line the process to achieve parallelism. This type of parallelism is asymmetrical because there could be unequal computation on the cores. However, the system can allocate several other tasks to unused instructions of a core to achieve load balancing and still maintain flexibility. **Figure 7** shows the data-flow model for a combination of line- and macroblock-processing frameworks.

In several other applications, data dependency would exist across multiple blocks of data. The data-access pattern is still predictable, but it extends beyond the granularities of a macroblock or a line. For example, a motion-window search uses several adjacent macroblocks. The data-access pattern is still predictable, but the system accesses blocks of data between several iterations of an algorithm. In such cases, you can modify the frameworks to achieve efficient parallelism. For example, if dependencies exist between several lines, you can modify the line-processing framework to transfer slices of frames of N sequential lines to the L1 memory of each core. In a similar way, you can extend the macroblock-processing framework to transfer more than one macroblock to the internal L1 memory from the L2 memory.

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FRAMEWORK ANALYSIS

To evaluate the dual-core frameworks, Analog Devices first developed a single-core application with the data-flow model and then compared it with the dual-core implementation. **Reference 1** discusses the single-core models in more detail. Blackfin-specific system-optimization techniques can also efficiently use the available bandwidth (**Reference 2**). To keep the analysis simple, the company compared only the speed of the basic frameworks and not the combination of frameworks.

The cycles are the core computation cycles available for processing the stream data to meet real-time constraints for an NTSC (National Television Systems Committee) video input. For a core running at 600 MHz, the total cycles available per pixel to meet the real-time constraints is 44 cycles/pixel. Any core access to the stream data is only a single-core cycle, as all data access is to L1 memory. The cycles shown also exclude any interrupt latency.

As **Table 1** shows, the dual-core frameworks effectively double the speed on all the frameworks. The **table** also shows the L1-memory usage for each core and the shared-memory space that each framework requires. The frameworks use the Analog Devices DD/SSL (device driver/system services library) for peripheral and data management (**Reference 3**). EDN

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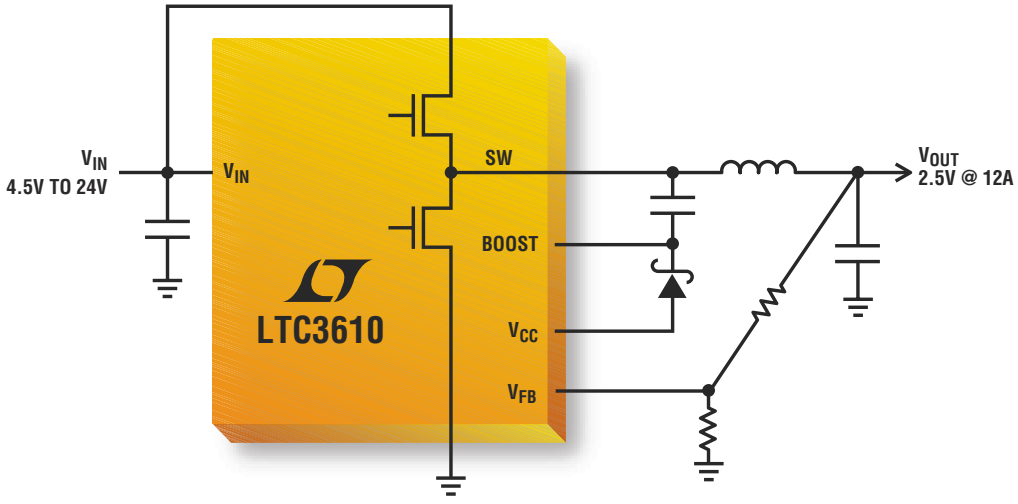

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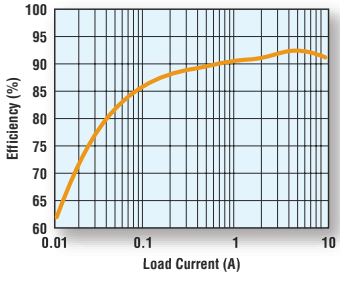

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AUTHORS' BIOGRAPHIES

Kaushal Sanghai has been a Blackfin applications engineer at Analog Devices since 2006. He holds a master's degree in electrical engineering from Northeastern University (Boston) and a bachelor's degree in electronics engineering from Mumbai University, India. His areas of interest include embedded-system design, computer architecture, and parallel computing.

Rick Gentile joined Analog Devices in 2000 as a senior DSP-applications engineer, and he currently leads the processor-applications group. He is co-author of Embedded Media Processing. *Before joining Analog, Gentile was a member of the technical staff at the Massachusetts Institute of Technology Lincoln Laboratory, where he designed several signal processors for a range of radar sensors. He has a bachelor's degree from the University of Massachusetts—Amherst and a master's degree in electrical and computer engineering from Northeastern University (Boston).*

David Katz has more than 15 years of experience in analog, digital, and embedded-system design. Currently, he is Blackfin applications manager at Analog Devices, where he is involved in specifying and supporting processor-based embedded designs. He is co-author of Embedded Media Processing. *Previously, he worked at Motorola as a senior design engineer in cable-modem and automation groups. Katz holds both bachelor's and master's degrees in electrical engineering from Cornell University (Ithaca, NY).*

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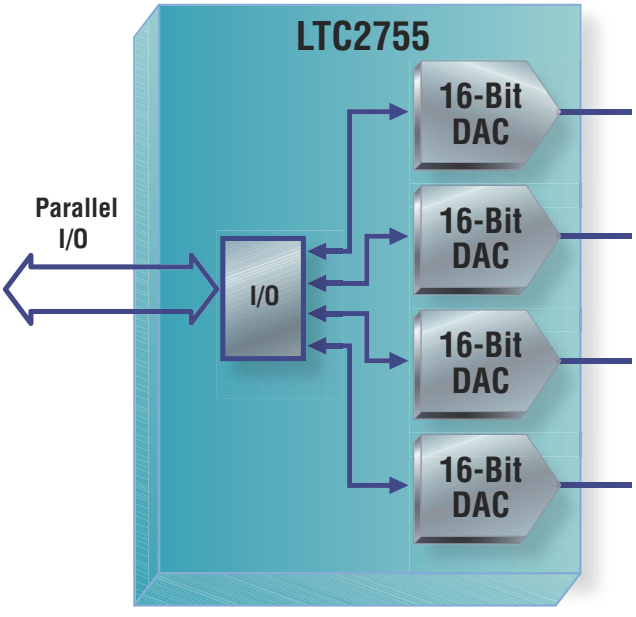

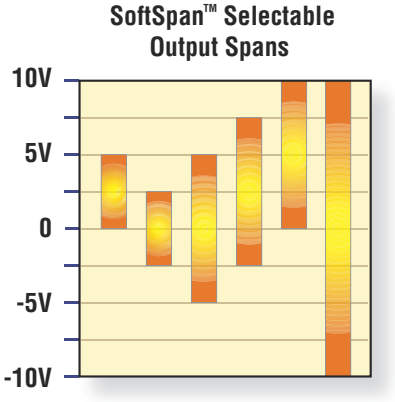

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LTC2755-12	12-Bits	4
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LTC2753-14	14-Bits	2
LTC2753-12	12-Bits	2
LTC2751-16	16-Bits	1
LTC2751-14	14-Bits	1
LTC2751-12	12-Bits	1

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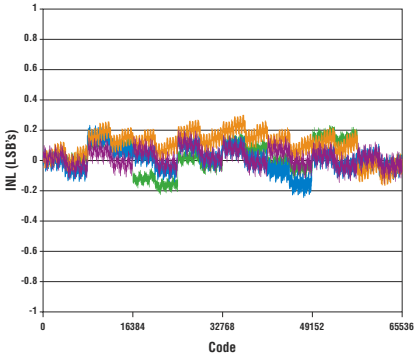

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Capacitive touch switch uses CPLD

Rafael Camarota, Altera, San Jose, CA

Capacitive touch switches work by measuring the change in capacitance of a PCB (printed-circuit-board) pattern depending on the placement of a user's finger over a sensing pad. Capacitive switches are becoming popular because they are less expensive than mechanical switches. Using the features of an Altera (www.altera.com) MAX IIZ CPLD (complex-programmable-logic device), you can implement a touch-switch decoder with no external components. The touch sensor employs an 8-mm-diameter sensing pad on the PCB using the solder mask as a dielectric. The circuit decodes a single switch, but you could use the approach for multiple switches, and it has programmable sensing thresholds that allow for different PCB layouts and dielectrics.

Figure 1 shows a simple circuit with no external components other than the capacitive-switch layout on the PCB. A basic touch-switch PCB layout is on the left. It comprises only an 8-mm copper circle surrounded by copper that connects to ground. The dashed line shows that the center sensor connects to the CPLD using a via and a backside copper trace. A solder mask acting as a dielectric covers the center sensor and ground. The PCB touch sensor becomes a variable capacitor, C_{TOUCH}.

The variable capacitor is part of a relaxation oscillator. The CPLD has a built-in weak pullup resistor on each I/O pin. C_{TOUCH} and the weak pullup resistor create an RC circuit. If the PINOSC (pin-oscillator) signal is low, the I/O pin will be low, making the D input to the PINOSC LPM (library-of-parameterized-modules) register low. LPM blocks come from the Quartus II LPM.

The register and other logic in the circuit use a free-running, 4.4-MHz internal oscillator, ALTUFM oscillator, as a clock. On the rising edge of the clock, PINOSC goes low, making the buffer-driving pin go to a high-impedance state. The weak pullup resistor slowly makes the pin voltage rise based on an RC time constant. Not touching the switch causes it to have the lowest capacitance and fastest rise time. Touching the switch causes it to have the highest capacitance and the slowest rise time. The pin-I/O buffer uses the Schmitt-trigger option of the CPLD to reduce the noise sensitivity of

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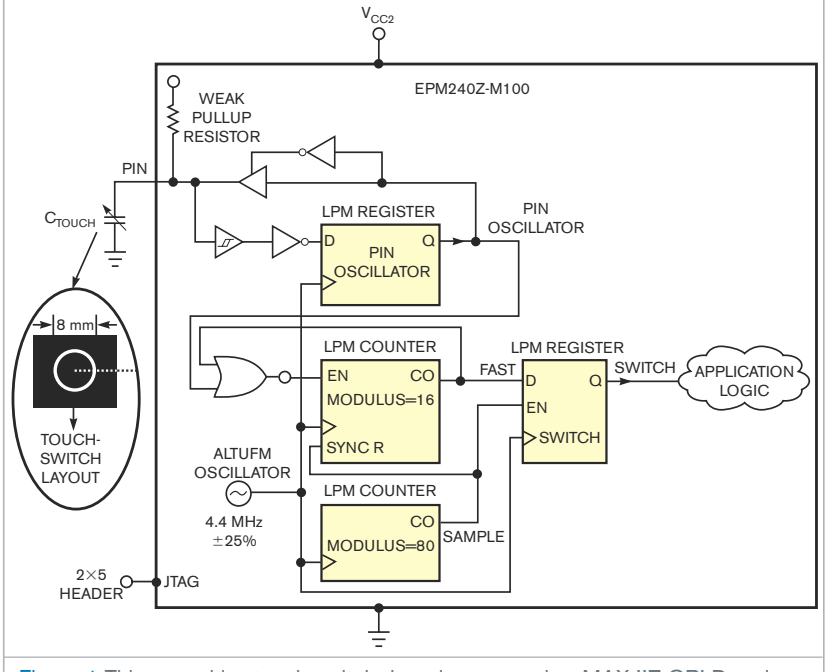

Figure 1 This capacitive-touch-switch decoder uses only a MAX IIZ CPLD and no external components other than the capacitive switch.

the slow-rising pin signal. Once the pin node reaches the high-voltage threshold, the D input of the PINOSC registers a zero. On the next clock edge, the PINOSC signal goes low, driving the pin node low for one full clock cycle. This PINOSC circuit oscillates at two fundamental frequencies, depending on the state of the touch capacitor. Putting the register into the oscillator loop reduces noise and makes the oscillator stable and synchronous with the decoding logic. The PINOSC period is always a multiple of 1/4.4 MHz or the frequency of the internal oscillator.

The switch decoder counts the period of 16 PINOSC cycles and compares it with a known time period. If 16 or more cycles happen in less than the sample period, it means that no one is touching the switch. If fewer than 16 cycles happen in the sample period, it means that someone is touching the switch, and the PINOSC oscillation becomes slower. The lower LPM counter sets the sample period.

For example, the sample signal was active once every 80 clock cycles in a prototype (**Figure 2**). The upper LPM counter measures the period of 16 PINOSC cycles. After 16 cycles, the fast signal goes high and stays high until the sample signal resets it. The fast signal is a one in the prototype when 16 cycles occur in fewer than 80 cycles, making the fast signal a one when the sample signal is a one. When the sample signal is a one, the fast value clocks into the switch-LPM register. The switch-signal value updates every sample cycle with the current capacitive switch state. When you touch the switch, PINOSC is slow, and the fast signal remains a zero when the sample signal is a one, making the switch output zero. In the prototype design, the PINOSC period was three clock cycles when someone touched it and nine cycles when no one touched it. The switch threshold was five cycles. Therefore, the lower LPM-counter modulus was 5×16=80. You can use any value from four to eight, but four is too sensitive, and eight does not work for small fingers; hence, five is the best value. The upper LPM-counter modulus affects noise sensitivity. The larger the count, the more the circuit averages the period of oscillation. A low modulus makes the circuit more sensitive to random system noise. The five-cycle sensing point also allows margin for the ±25% variation among parts of the internal oscillator frequency.EDN

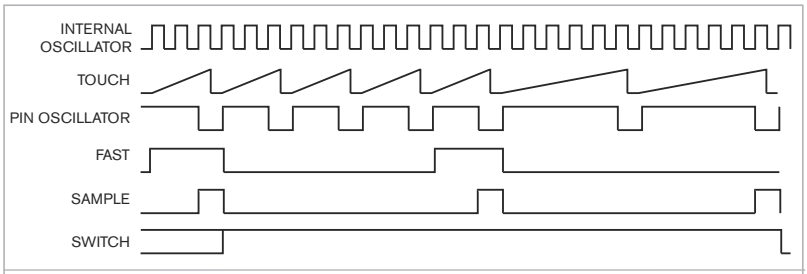

Figure 2 Representative waveforms that Figure 1 illustrates have a top-counter modulus of 3; a bottom-counter modulus of 12; and pin-oscillator periods of 3 and 6, respectively.

Bit-shifting method performs fast integer multiplying by fractions in C

Aaron Lager, Panamax Furman, Santa Rosa, CA

This Design Idea presents a method for fast integer multiplying and multiplying by fractions. What can you do when you lack access to a hardware multiplier or MAC (multiply/accumulate) function and you need to multiply by something other than a power of two? One option is to include the math.h function and just sling around the multiplication operator and watch your code bloat and slow to a crawl. Option two is to get fancy with bit shifting. The general idea is to find powers of two, including zero, that you can add to achieve the multiplier you need. This method works because of the distributive properties of multiplication. Using the distributive properties of multiplication, you can, for example, rearrange the problem of: 12×12=144→(4+8)×12=144→(12×4)+(12×8)=144. This version is amenable to implementation in C code because four and eight are powers of two. To implement the multiplications, you use the exponent of the power-of-two representation for your code as an integer shift. Because $4=2^2$ and $8=2^3$, you use two and three as your shift factors.

For example, multiply the variable foo by 12 to get 144: BYTE foo=12: foo=((foo<<3)+(foo<<2)). Left-shifting by three is the same as multiplying by eight, and left-shifting by two is the same as multiplying by four. Another example is multiplying by six: 6×10=60→(2+4)×10=60→(2×10)+(4×10)=60. BYTE foo=10; foo=((foo<<1)+(foo<<2)). Left-shifting by one is the same as multiplying by two, and left-shifting by two is the same as multiplying by four.

Using this same theory of distribution, you can also perform fractional multiplication or division. This method creates rounding errors just like dividing integers by values that are not powers of two does with math.h functions and the division operator.

One example is 2.5×10=25→(2+0.5)×10=25→(2×10)+(0.5×10)=25. The result is ((foo<<1)+(foo>>1)). Left-shifting by one is the same as multiplying by two, and right-shifting by one is the same as dividing by two or multiplying by 0.5. Another example is

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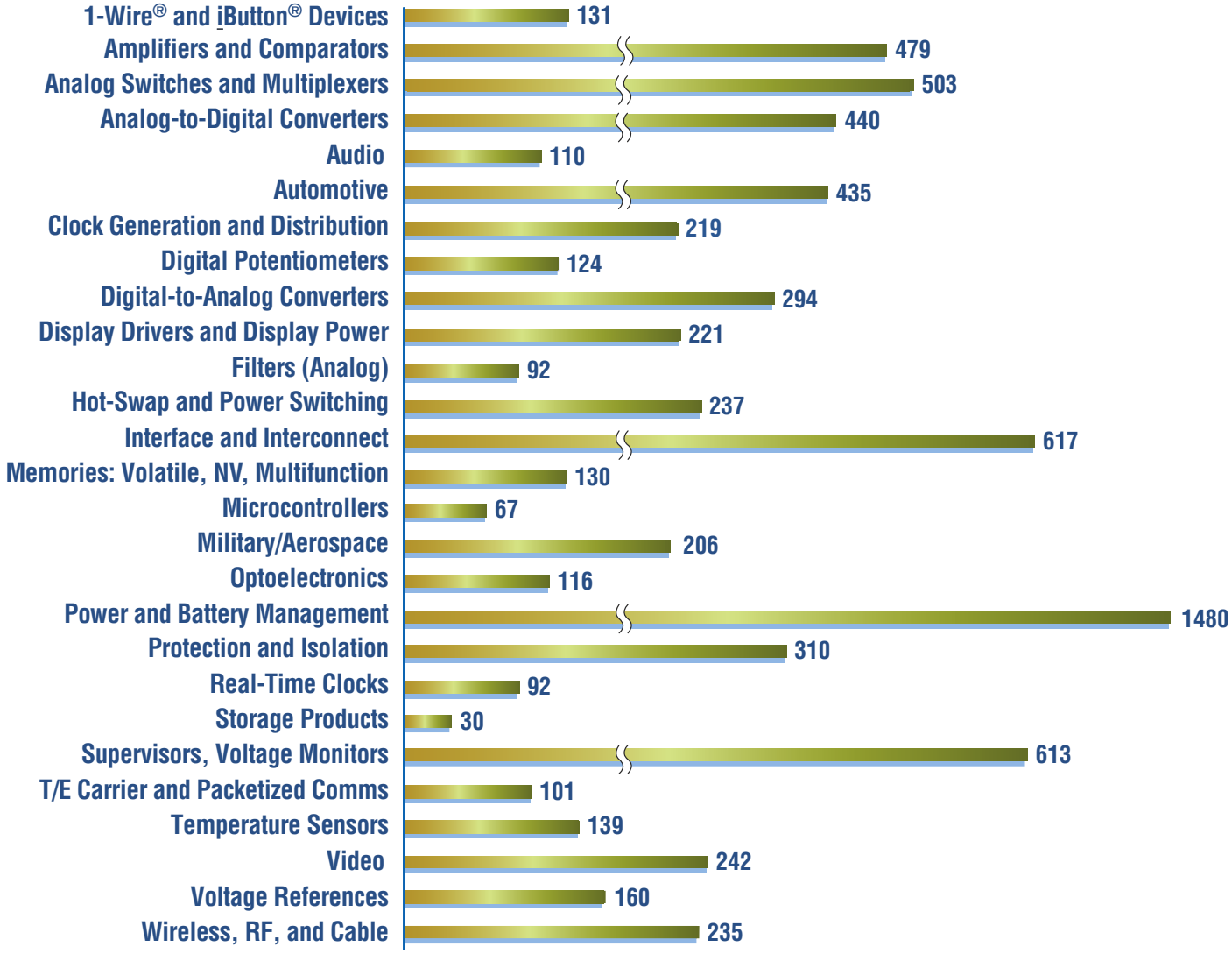

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3.125×80=250→(2+1+0.125)×80=250→(2×80)+(1×80)+(0.125×80)=250. The result is ((foo<<1)+foo+(foo>>3)). Left-shifting by one is the same as multiplying by two, multiplying by one is the same as adding the multiplicand once to the result, and right-shifting by three is the same as dividing by eight or multiplying by 0.125. A third example is 2.625×80=210→(2+0.5+0.125)×80=210→(2×80)+(0.5×80)+(0.125×80)=210. The result is ((foo<<1)+(foo>>1)+(foo>>3)). Left-shifting by one is the same as multiplying by two, right-shifting by one is the same as dividing by two or multiplying by 0.5, and right-shifting by three is the same as dividing by eight or multiplying by 0.125.

All of these examples take up less space and are faster than calling the standard 8×8-multiply function or division function from most standard math libraries. Also, you should note that, if the result of the variable you are multiplying can ever exceed 8 bits, then you should use a word function that can store 16 bits of your result, and you should use casting on the outer parentheses. The result is (word)((foo<<1)+(foo>>1)+(foo>>3)).EDN

RS-232-to-TTL converter tests UARTs with a PC

Matthieu Bienvenüe, Malissard, France

You often need an RS-232-to-TTL adapter for debugging or testing UARTs using a computer. But most of these adapters require an external power-supply adapter to power up the RS-232 transceiver. This external adapter increases the number of cables on your desk and uses no flow-control signals. This Design Idea describes how you can use these signals as power sources. It uses the RTS (request-to-send) and DTR (data-terminal-ready) signals, which provide a positive voltage when you open the PC's COM port (**Figure 1**). The voltage on those pins can differ from one computer to another but is generally higher than 6V, which is sufficient to power the adapter.

A standard RS-232 MAX3232 line driver from Maxim (www.maxim-ic.com) performs the TTL-to-RS-232 conversion. The MAX3232 accepts a 5 or 3.3V supply voltage, which is switch-selectable using S_1. D_1 and D_2 block the negative voltage that occurs when the COM port is closed. Q_1, R_3, S_1, and zener diodes D_3 and D_4 form a simple voltage regulator. LED_1 signals that the COM port is open. R_1, R_5, and R_6 protect the circuit under test and the line driver. The use of a pull-up resistor for R_2 avoids the need for an open input. This circuit has successfully undergone testing with a laptop computer, which provides a 6V power supply. The circuit works well at speeds as high as 115,200 bps.EDN

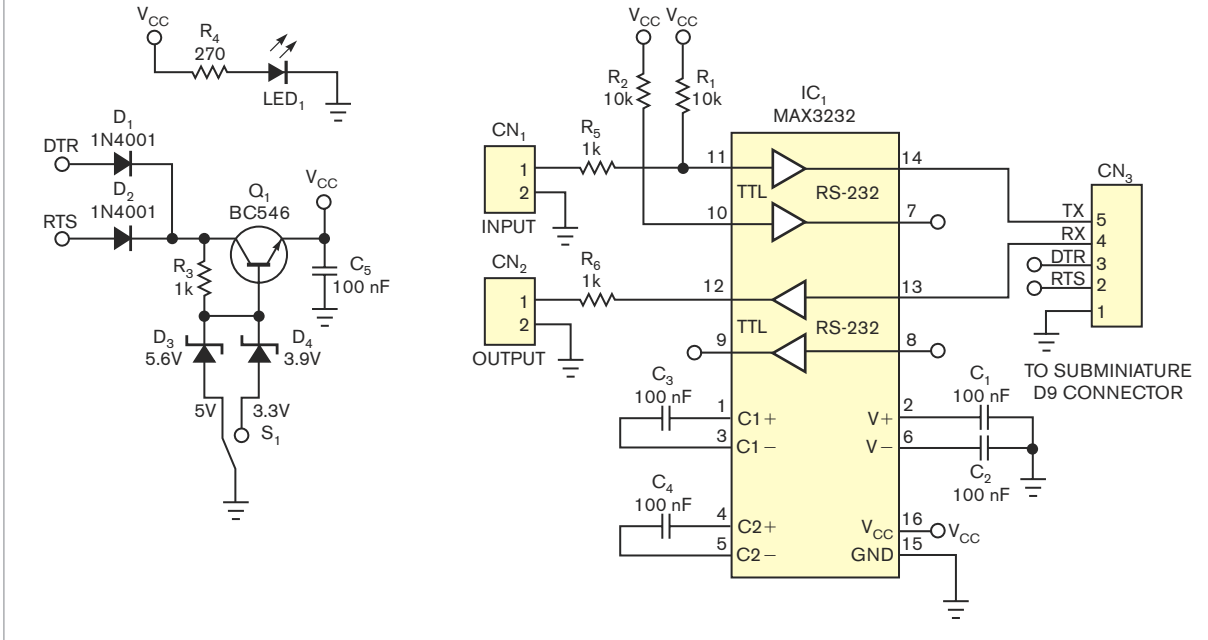

Figure 1 An RS-232-to-TTL converter uses the unused DTR and RTS outputs of a PC's COM port to self-power the circuit.

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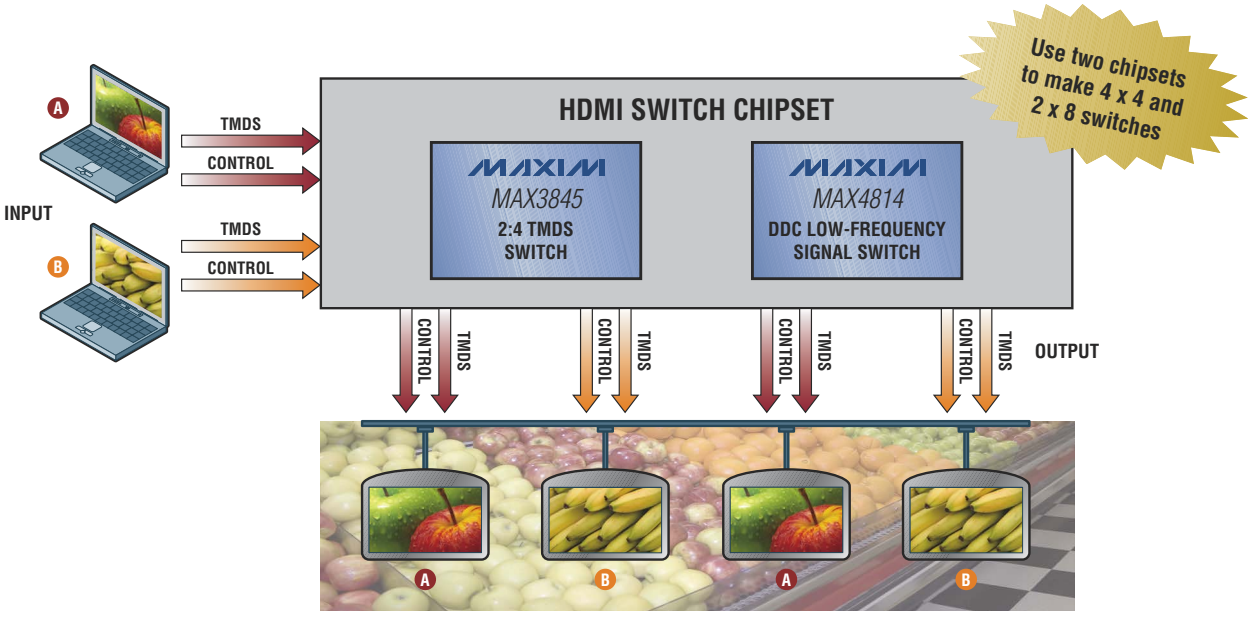

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Hot-swap circuit allows two computers to monitor an RS-232 channel

Jeff Patterson, All Weather Inc, Sacramento, CA

The hot-swap serial-interface circuit in **Figure 1** allows two computers to see all of the communication between each computer and each device on the communication network for that serial port. This circuit allows each computer to determine what the other is doing and receive all of the data from the peripheral device. Only one device can transmit at a time; otherwise, the transmitted data becomes corrupted. This circuit allows two computers in a hot-swap configuration to know when to become the master computer. When the master computer fails, the slave computer stops receiving the data requests that the master supplies, and the slave then becomes the master. This approach allows for computer redundancy in applications in which a master computer that is communicating with an RS-232 device must always be operating. When you replace the failed computer, it "hears" that a master computer is communicating with the device and operates in slave mode while waiting for the current master to fail.

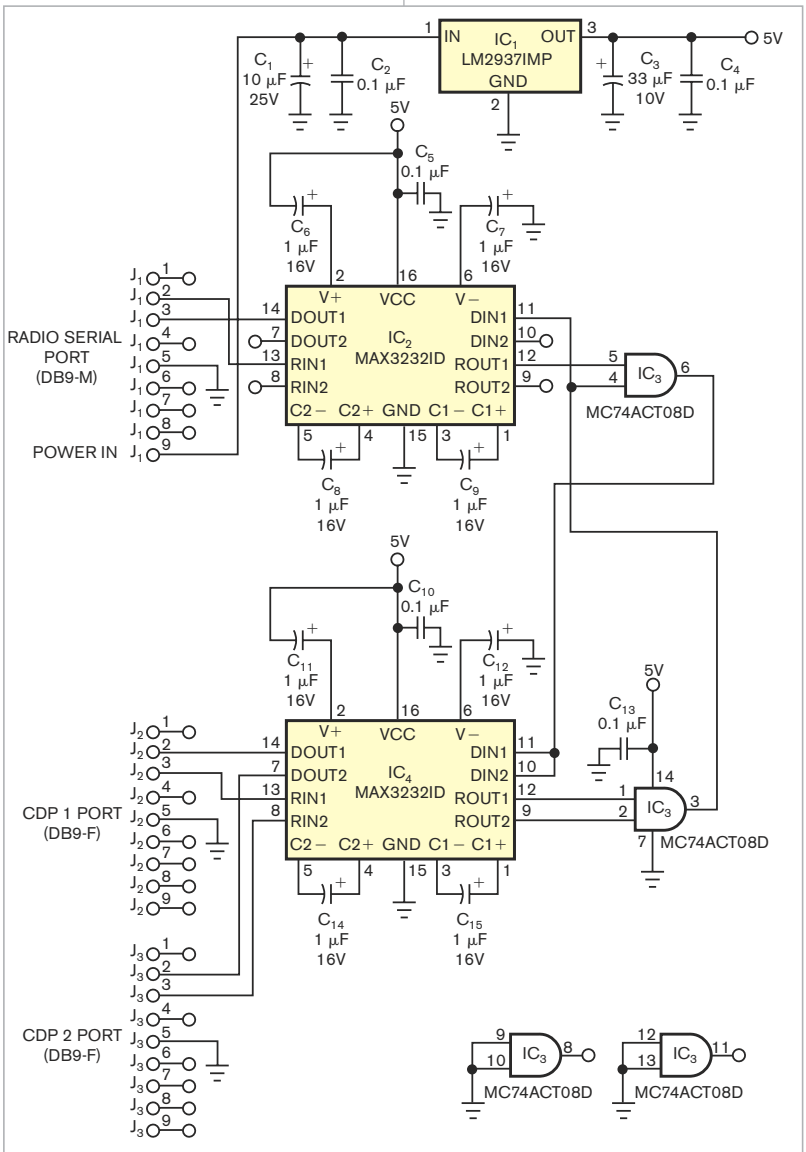

Figure 1 This hot-swap RS-232 interface allows two computers to monitor traffic on a computer's RS-232 port.

This circuit allows two DTE (data-terminal-equipment) computers to use one DCE (data-communications-equipment) RS-232 peripheral device. This device is usually a communication interface, such as a UHF radio or an RS-232-to-RS-485 converter. The board requires 9 to 15V dc to operate. You must provide this voltage on Pin 9 of the peripheral RS-232 device.

The transmitted RS-232 signal from the peripheral device converts to a TTL signal through level converter IC_2 and feeds into an AND gate. The output of this AND gate feeds into two inputs of another level converter, IC_4. These RS-232 outputs travel to the input lines (Pin 2) of the two monitoring computers. When one of the computers transmits on Pin 3 of its serial port, its output converts to TTL levels with IC_4. The TTL-converted outputs of both computer serial ports feed into an AND gate. The default, or off, level for a computer serial port is −12V dc. The level converter inverts the signal as part of the conversion to TTL levels. This action makes the default a high level going to the AND gate, allowing the data on the other input of the AND gate to pass to the output of the AND gate.

The output of this AND gate goes to the second input of the AND gate that receives the output of the peripheral device as well as the input into the level converter going to the input of the peripheral device at Pin 3. This action enables the output of one of the two computers to return to the computer that transmitted the data as well as to the other computer and the peripheral device. EDN

Lowest power key-switch controller for portable applications

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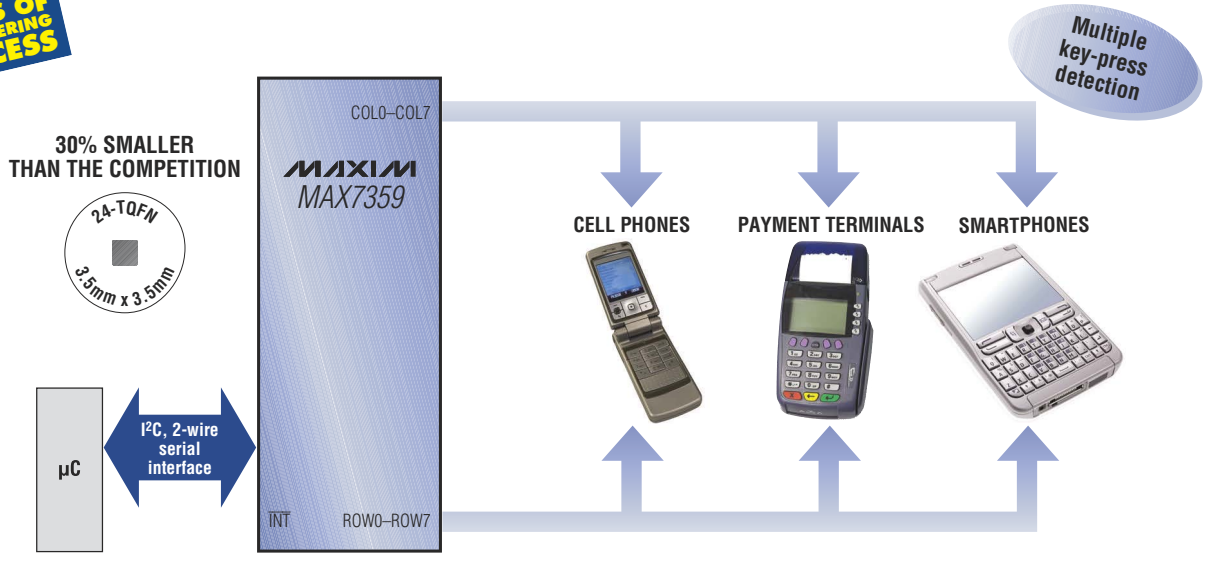
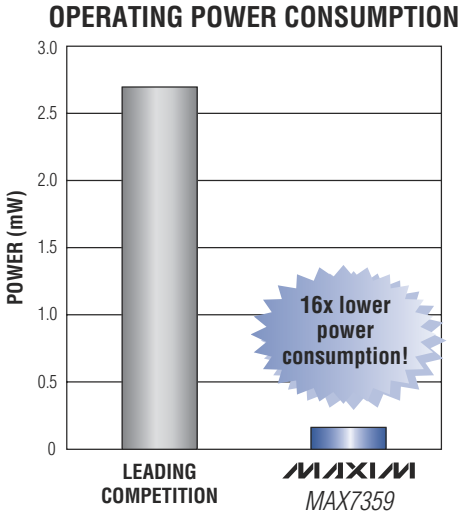
The MAX7359 key-switch controller monitors and debounces press and release activity on up to 64 keys. This device reduces total system cost by simplifying software development and eliminating external components.



Key Features

- Low, 1.62V to 3.6V supply-voltage range
- Key-release detection on all keys
- Integrated ghost-key elimination
- Column drivers configurable as GPOs
- Small, 3.5mm x 3.5mm TQFN package



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Improved laser-diode-clamp circuit protects against overvoltages

James Zannis, Baulne-en-Brie, France

Expensive semiconductor laser diodes have no tolerance for fast voltage or current transients. To minimize the risk of damage, a standard JFET-clamp circuit shorts the laser when there is no supply voltage, thus protecting it against such transients (**Figure 1**). When the negative supply rail comes up, the JFET turns off. This circuit is effective for low-power laser diodes but may not be so for diodes with power dissipation greater than 150 mA. The maximum cutoff current of the JFET sets this limit. If it becomes necessary in an emergency to clamp the laser during normal operation, the selected JFET might not adequately shunt the current. Higher-current JFETs are available but are more expensive and difficult to procure.

The circuit in **Figure 2** avoids these deficiencies. It is similar to the standard JFET circuit but has a supplementary bipolar transistor that shunts most negative-going currents when the JFET is on. R_2 prevents the gate of Q_1 from floating, and R_3 ensures rapid turn-off of Q_2. The 1N914 diode bypasses any positive-going transients. The RC circuit ensures an adequately slow response; therefore, the transition between on and off is smooth. EDN

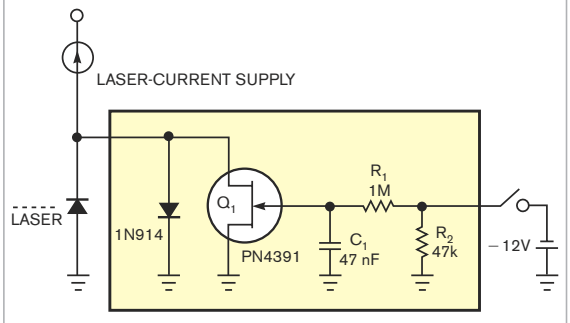

Figure 1 This circuit protects low-power laser diodes but is not suitable for higher-power laser diodes.

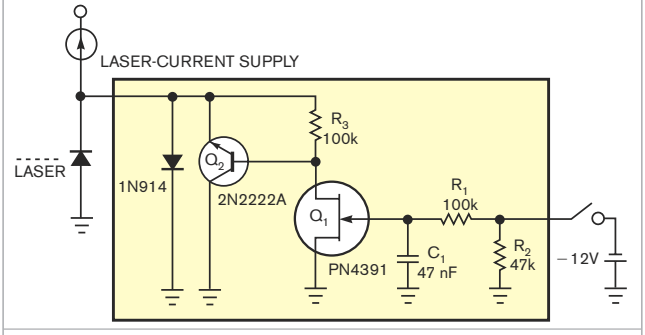

Figure 2 Adding a bipolar transistor to the circuit in Figure 1 allows the circuit to protect higher-power laser diodes.

LINEAR TECHNOLOGY

DESIGN NOTES

Compact I²C-Controllable Quad Synchronous Step-Down DC/DC Regulator for Power-Conscious Portable Processors

Design Note 442

Jim Drew

Introduction

The LTC®3562 quad output step-down regulator is designed for multicore handheld microprocessor applications that operate from a single Li-Ion battery. Its four monolithic, high efficiency buck regulators support Intel's mobile CPU P-State and C-State energy saving operating modes. The output voltages are independently controllable via I²C, and each output can be independently started and shut down. Designers can choose from power saving pulse-skipping mode or Burst Mode® operation, or select low noise LDO mode. The space-saving LTC3562 is available in a 3mm × 3mm QFN package and requires few external components.

Four I²C-Controllable Regulators

Two of the regulators provide up to 600mA of output current each while the other two provide up to 400mA each. All regulators are internally compensated, so no external compensation components are needed.

One of the 600mA regulators and one of the 400mA regulators (R600A and R400A) feature I²C-controllable feedback voltages, as shown in Figure 1. The output voltages of these "Type A" regulators are set by a combination of external programming resistors and I²C-adjustable feedback voltages—16 settings from 425mV to 800mV.

The "Type B" regulators (R600B and R400B) do not require external programming resistors because the resistors are integrated on-chip. The values of the internal feedback resistors are adjusted through the I²C port, resulting in 128 possible output voltages from 600mV to 3.775V in 25mV increments.

Inrush current limiting is provided by soft-start circuitry in all four regulators, as well as short-circuit protection and switch node slew rate limiting to reduce EMI.

Power Saving Operating Modes

The LTC3562's step-down regulators offer four selectable modes of operation, which make it possible to balance low noise against efficiency. The four operating modes of the LTC3562 are shown in Figure 2.

At moderate to heavy loads, the constant frequency pulse-skipping mode provides the best output switching noise solution. At lighter loads, either Burst Mode operation or forced Burst Mode operation can be selected to maximize efficiency, though these modes produce higher ripple.

If the application calls for the lowest possible noise, LDO mode can be used for up to 50mA of load current.

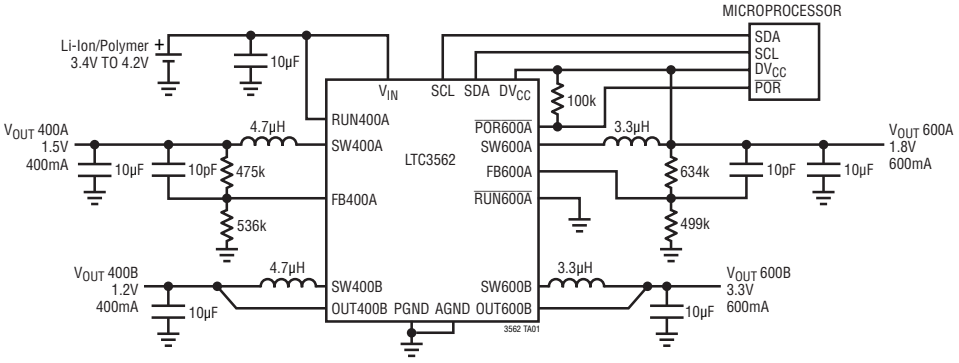

Figure 1. High Efficiency Quad Step-Down Converter with I²C Control

All four converters support 100% duty cycle operation when the input voltage drops very close to the output voltage setting.

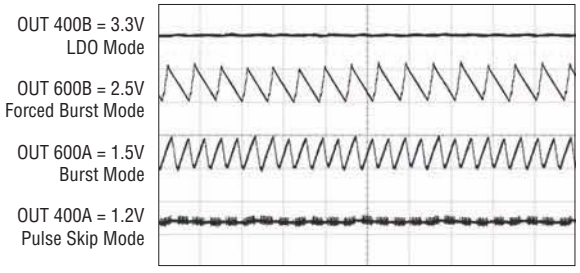

Figure 2. Modes of Operation

I²C Programming of Output Voltages Allows Easy Sequencing, Tracking and Margining

Each output can be programmed on the fly and independently enabled or disabled. These features taken together enable almost any sequencing or tracking scheme. A sequencing example is shown in Figure 3.

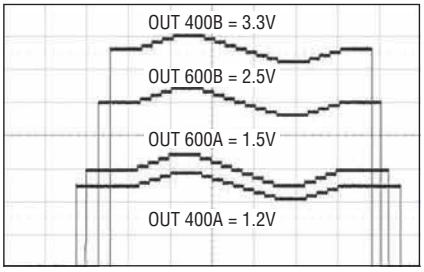

Figure 3. LTC3562 Voltage Sequencing and Margining

A coincident voltage tracking example is shown in Figure 4. All of the outputs are ramped up together at power up. At power down, the highest output is incrementally ramped down until it reaches the value of the next higher voltage, which ramps down with the first. This is repeated until each output has tracked down to a minimum value and then disabled.

The ability to adjust the output voltage on the fly is also useful to margin the supplies for design evaluation or manufacturing quality audit testing. Voltage margining is applied to the nominal operating voltages in Figure 3 and Figure 4.

Reducing the voltage or shutting down any output can reduce battery life or reduce energy usage in 'green' applications.

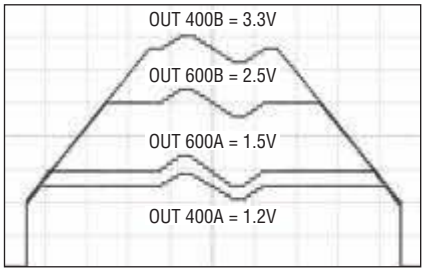

Figure 4. LTC3562 Voltage Tracking and Margining

Conclusion

The LTC3562 is a versatile high efficiency quad output monolithic synchronous buck regulator controlled with an I²C interface in a 3mm × 3mm QFN package. Four modes of operation allow the switching regulators to be tailored to the system's efficiency and noise requirements. This device is well suited for handheld microprocessor applications operating from a single Li-Ion battery where battery life is critical. The ability to use I²C to adjust output voltages on the fly or disable output voltages supports Intel's mobile CPU P-State and C-State energy saving modes of operation and simplifies development and manufacturing tolerance testing.

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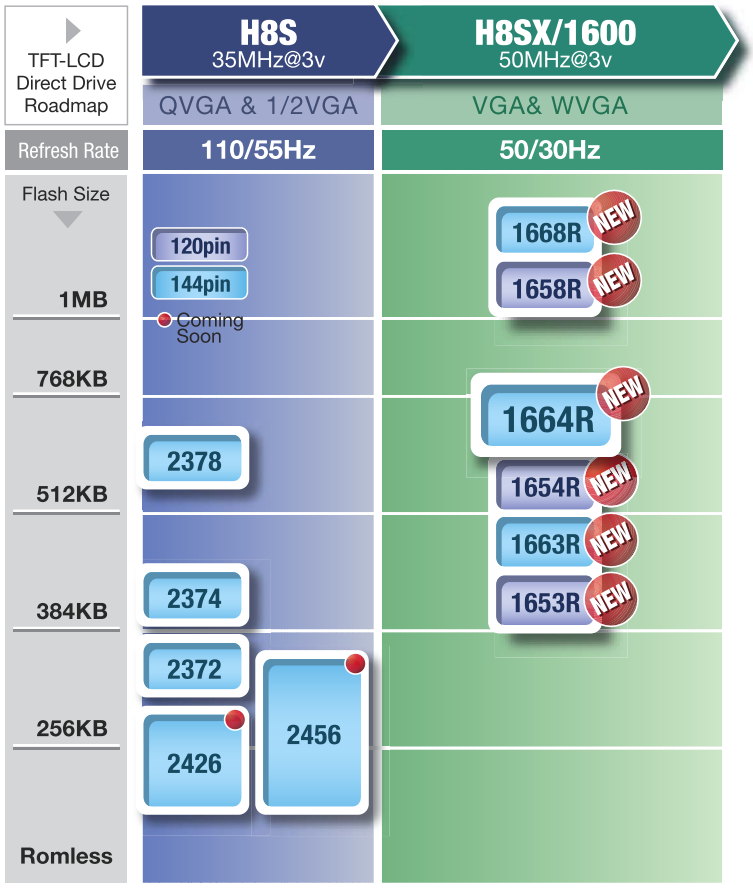
H8SX Product Lineup



HOT Products | **H8SX/1664R**

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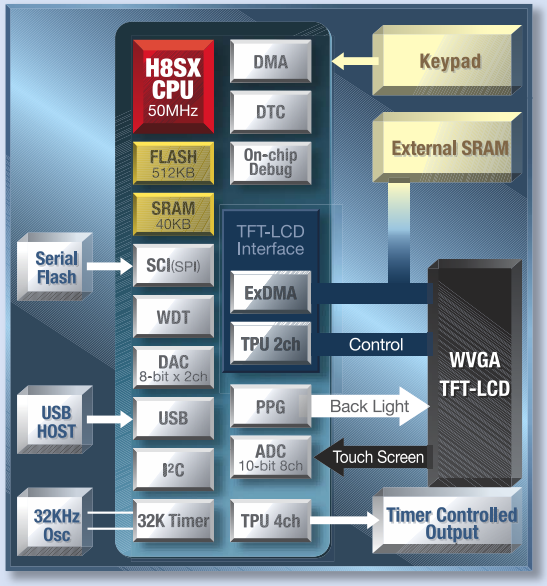

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  - 32KHz clock input with timer
  - Full Software API with complex LCD images supported
  - Driver source code, full documentation, demos
  - Several connectivity interfaces; e.g., USB, serial interfaces, I²C-BUS

*Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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BY SUZANNE DEFFREE

supplychain

LINKING DESIGN AND RESOURCES

Auction-style site aims to thwart gray market

Looking to counter the gray market's counterfeit-component issues, an online electronics-supply-chain service is aiming to bring together chip manufacturers, OEMs (original-equipment manufacturers), CEMs (contract-electronics manufacturers), and franchise distribution into an auction-style community. "We are dealing with the top 25 CEMs and OEMs," says Richard Tapping (**photo**), general manager of the online-services tool, Semicentral.com. "What we've tried to do here is create a circle of companies, and the only way a product can get into [the circle] is through an authorized or factory-supply chain."

The tool enlists no membership or listing fees. Similar to other auction sites, such as eBay, Semicentral.com takes a 10 to 20% commission on sale prices, which the component seller controls. Buyers and sellers remain anonymous and are identified by numbers. A rating system allows user comments to qualify users.

Semicentral.com does not aim to compete with distributors. In fact, it came out of the gate on May 5 with Arrow Electronics Inc among its supporters. Instead, the tool aims to offer an applicable service to the electronics supply chain for the trade of excess inventory and looks to its users to ensure against counterfeit products. Tapping admits that the site cannot offer a 100% guarantee that traded components are not counterfeit. However, he says that, unlike gray-market flow, Semicentral.com will remove any such product and its respective participant. That approach, he believes, will offer the electronics supply chain a safer way to buy and sell excess inventory than using gray-market sources.

"It's recognized that something needs to be done; it needs to be done by the community. There is no reason, ultimately, for an OEM or a CEM in today's market to buy from a gray-market channel if they have the right tools to be able to give them the visibility of masses of inventory," Tapping concludes.

GREEN UPDATE

EPA WORKS WITH THE GREEN GRID ON ENERGY EFFICIENCY

The EPA (Environmental Protection Agency, www.epa.gov) has turned the microscope on itself, last month announcing that it will begin to evaluate its computer rooms for ways to optimize energy efficiency and then will find ways to standardize processes and performance measures. In doing so, the government arm has signed a memorandum of understanding with data-center energy-efficiency consortium The Green Grid (www.thegreengrid.org) to promote energy efficiency in its small computer rooms.

The EPA plans to share its best practices for replication with other governmental agencies and industry stakeholders and expects that future partnerships will help design and build a green federal-IT infrastructure. The initiative will likely mandate stricter energy-efficiency designs for vendors that play in the federal-electronics-supply chain.

According to the EPA, computer rooms across the United States accounted for 1.5% of total US electricity demand in 2006, equal to the annual electric consumption of the state of Florida. "Throughout the United States, computer centers are becoming the fastest growing users of energy. As this sector experiences tremendous growth, EPA and The Green Grid see tremendous opportunity," says EPA Administrator Stephen L Johnson. "By investing in energy efficiency in our own computer centers, we are proving that doing what's good for the environment is also good for the bottom line."

OUTLOOK

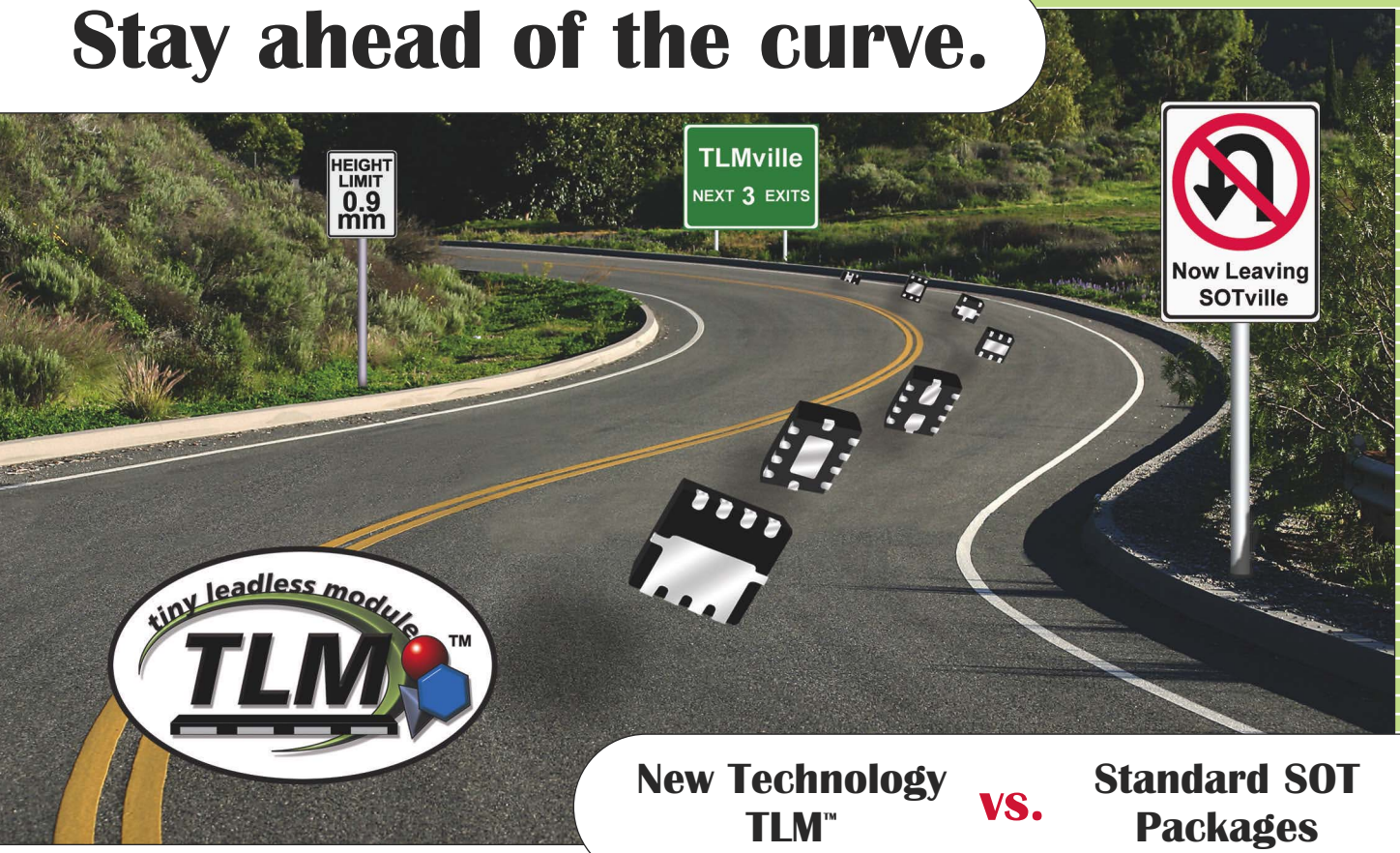
LED SHIPMENTS TO CLIMB ON NOTEBOOK USAGE

LEDs will light the notebook-PC-display-backlighting market ablaze during the next few years, with iSuppli Corp (www.iSuppli.com) predicting that nine out of 10 large mobile-PC LCD panels will use the technology by 2012. The market-research company estimates that 90% of large LCD-notebook-PC panels manufacturers ship in 2012 will employ LEDs to backlight their displays, rocketing up from just 4.7% in the fourth quarter of 2007. LED-backlit large LCD-notebook-PC-panel shipments will surge to 17.4 million units by the end of 2008, up by more than a factor of six from 2007, the company forecasts. ISuppli defines large LCD panels as those having a diagonal dimension of 10 in. or more.

"Currently, LCDs in notebook PCs employ CCFLs [cold-cathode-fluorescent lamps] for backlighting," says Sweta Dash, director of LCD and projection research at iSuppli. "While this is a proven technology and has lower cost [than] LEDs, it faces shortcomings in power consumption and thickness compared to LEDs."

Accordingly, iSuppli reports that, as the cost differential between LED and CCFL backlights narrows, LED-based notebook-PC panels will gain market share.

Stay ahead of the curve.



New Technology TLM™ vs. Standard SOT Packages

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Designed for today's ultra thin electronic products, Central Semiconductor Corp. introduces the TLM™ (Tiny Leadless Module) family. The TLM™ packages feature lower profile (height) and utilize less board space as compared to standard SOT packages. Find below several featured devices from this new family:

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Central Type No.	I_F (A)	V_{RRM} (V)	Description	TLM Size L x W x H (mm)	Package
*CTLSH1-40M621H	1.0	40	Single, Schottky	2 x 1.5 x 0.4	TLM621H
CTLSH1-40M832D	1.0	40	Dual, Schottky	3 x 2 x 0.9	TLM832D
CTLSH2-40M832	2.0	40	Single, Schottky	3 x 2 x 0.9	TLM832
CTLSH3-30M833	3.0	30	Single, Schottky	3 x 3 x 0.9	TLM833
CTLSH5-40M833	5.0	40	Single, Schottky	3 x 3 x 0.9	TLM833

Transistors

Central Type No.	I_C (A)	V_{CBO} (V)	Description	TLM Size L x W x H (mm)	Package
*CTLT3410-M621	1.0	40	Low $V_{CE(SAT)}$, NPN	2 x 1 x 0.8	TLM621
*CTLT7410-M621	1.0	40	Low $V_{CE(SAT)}$, PNP	2 x 1 x 0.8	TLM621
CTLT853-M833	6.0	200	High Current, NPN	3 x 3 x 0.9	TLM833
CTLT953-M833	5.0	140	High Current, PNP	3 x 3 x 0.9	TLM833

Combo: Low $V_{CE(SAT)}$ Transistor and Low V_F Schottky Rectifier MDM

Central Type No.	Transistor		Rectifier		TLM Size L x W x H (mm)	Package
	I_C (A)	V_{CBO} (V)	I_F (A)	V_{RRM} (V)		
CTLM1034-M832D (NPN)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D
CTLM1074-M832D (PNP)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D

Central welcomes the opportunity to explore selected, special, or custom devices, upon request.

* Under Development

The TLM™ Advantage

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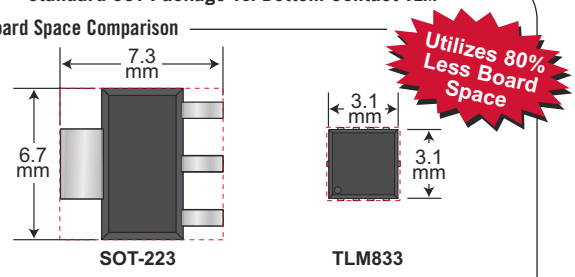

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productroundup

POWER SOURCES

24V dc/dc converters target vehicle-battery systems

New 24V devices in the vendor's VI-J00 and VI-200 dc/dc-converter families have a 10 to 36V input-voltage range, suiting applications operating from 12 or 24V inputs, typical for battery systems in vehicles. Measuring 4.6×2.2×0.5 in., the VI-200 model provides 16 output voltages ranging from 3.3 to 48V with a 75W maximum power. Devices in the VI-J00 series measure 2.28×2.4×0.5 in., offer 16 output voltages of 2.2 to 48V, and have 50W maximum power. Prices for the 24V-dc input VI-J00 and VI-200 models start at $89 (100).

Vicor Corp, www.vicorpower.com

Power adapter suits worldwide ac/dc needs

With a universal 90 to 264V-ac input, the 72W AD72 external ac/dc power adapter finds use in worldwide applications. The device produces a regulated 16V-dc output that delivers as much as 4.5A of continuous power. Complying with the Blue Angel requirement, the power adapter provides 84% typical efficiency. Features include a two-pin, type-C8 IEC320 ac-input receptacle, an internal ac-input fuse, and a 6-ft dc-output cable with a 2.1-mm right-angle barrel plug. The AD72 power adapter costs $35.

Emerson Network Power, www.emersonnetworkpower.com

20W, PCB-mountable ac/dc power supply comes in multiple output voltages

Accepting an 85 to 264V-ac-voltage range, the 20W ZPSA20 PCB (printed-circuit-board)-mountable ac/dc power supply come in 3.3, 5, 9, 12, 15, and 24V-dc output voltages. The device features floating outputs, allowing use as a positive or a negative polarity, 82% efficiency, and a 0 to 70°C operating temperature with derating. The device comes as an open-board configuration with Molex I/O connectors, or as a /P version with pins for PCB mounting. Measuring 2×3.5×0.79 in., the ZPSA20 power supply costs $12.50 (1000).

Lambda, www.lambdapower.com

Rectifier provides 12.5 kW per rack unit

Claiming 92% efficiency, the 2500W, 48V FMP25.48 rectifier has a 27W/in.^{3} power density, enabling 12.5 kW of power in a one-rack-unit, 23-in. shelf. Features include a 90 to 300V-ac input range, a high-input-voltage shutdown, and the ability to withstand a loss of phase or neutral without damage. The device is compatible with the vendor's Guardian dc-power series, which includes rack and cabinet systems delivering 500A with 720-Ahr backup-battery capability. The device supports medium and large power requirements with 1200A per bay at power as high as 6400A. Measuring 4.2×13.2×1.6 in., the FMP25.48 rectifier costs $425.

Power-One, www.power-one.com

CAN transceiver provides automotive power management

Targeting automotive-CAN (controller-area-network) applications requiring speeds as high as 1 Mbps, the MAX13041 transceiver provides an advanced interface between the protocol controller and the physical bus in a CAN node. Power-management features reduce power consumption in ECU (electronic-control-unit) modules that a battery permanently supplies. A ±80V fault-protected voltage range and

±12-kV human-body-model ESD protection on the CAN-bus lines suits the device for 12/42V automotive and truck applications. Suiting clamp-30, always-on nodes, the transceiver has five operation modes, providing reduced power consumption. The device completely powers down during sleep mode. During local or CAN-bus activity, the device enables the onboard voltage regulator, restoring power to the clamp-30 node, and it allows interrogation of wake-up-source recognition by the onboard microcontroller. The MAX13041 transceiver costs 89 cents (1000).

Maxim Integrated Products, www.maxim-ic.com

Switching regulator comes in miniature SIP package

The miniature SR7805 point-of-load switching regulator provides 7.5W of output power. Operating from 4.75 to 32V-dc inputs, the regulator provides 3.3, 5, 6.5, 9, 12, or 15V-dc outputs. Claiming a 96% efficiency, the device has a 2 million-hour MTBF (mean time between failures). Using free-air-convection cooling allows a −40 to +85°C temperature range, and the device requires no derating or heat sinking. Additional features include low-noise operation and tight line/load regulation. Available in a 0.45×0.3×0.4-in. miniature-SIP package, the SR7805 switching regulator costs $5.55.

MicroPower Direct, www.micropowerdirect.com

INTEGRATED CIRCUITS

Stereo-audio processor supports Bluetooth

Targeting use in mobile phones, the single-chip MusiCore1 stereo-audio processor reduces the cost of an audio processor by 75%, according to the vendor. The device, with a 36-mm^2 footprint, has a 95-dB SNR (signal-to-noise ratio) and 30-dB dynamic-background-noise reduction. It uses BlueCore technology, providing support for Version 2.1+EDR (enhanced-data-rate) Bluetooth and the vendor's FastStream 40-msec-latency Bluetooth technology. Available in 3.8×4.8-mm CSP or BGA packages, the ROM version of the MusiCore1 stereo-audio processor costs $4 (100,000).

CSR, www.csr.com

Audio ICs support digital- and analog-baseband audio

The flexible ADAV4601 and ADAV4622 programmable audio ICs combine an integrated broadcast-audio processor and an ASD (auto-standard-detecting) processor. The ICs support digital- and analog-baseband

productroundup

INTEGRATED CIRCUITS

audio, as well as multistandard analog-broadcast demodulation and decoding for worldwide broadcasting standards, including BTSC (Broadcast Television Systems Committee), EIAJ (Electronics Industries Association of Japan), A2-Korea, A2-Europe, and NICAM (near-instantaneous companded audio multiplex). The audio processors feature a dedicated TV-audio flow using full-matrix switching from any input to any output; automatic volume control, compensating for volume changes during advertisements or switching channels; dynamic bass; a multiband equalizer; and a 200-msec stereo-delay memory for audio/video synchronization. Available in 14×14-mm pin-for-pin- and software-register-compatible LQFPs, the ADAV4601 and ADAV4622 cost $3.85 and $4.75 (10,000), respectively.

Analog Devices, www.analog.com

Audio DAC features playback-time-extender technology

Requiring no voltage regulator, the 24-bit STw5210 audio DAC directly connects to the battery. Providing playback-time-extender technology, the devices has a 103-dB SNR (signal-to-noise ratio). The converter features line and headset outputs suiting mobile music handsets. Packages include the 2.6×2.6×0.6-mm WLCSP36 with a 0.4-mm pitch and the 4×4×1.2-mm TFBGA40 with a 0.5-mm ball pitch. The STw5210 audio DAC costs $1.80 (1000).

STMicroelectronics, www.st.com

Expander provides 24 configurable general-purpose I/O ports

Targeting use in mobile peripheral devices, the TC35892XBG flexible I/O expander offers as many as 24 configurable, general-purpose I/O ports at needed locations. The device integrates keypad management, PWM (pulse-width-modulation)-signal generation for LED and vibrator control, and a rotator-wheel interface. Additional features include a 1.7 to 2.7V power-supply range; two power modes; voltage supplies for as many as three I/Os; a watchdog function; and failsafe operation for I^2C, interrupt, reset, and clock. The expander provides an internal clock generator, and allows operation from a 32-kHz low-frequency clock source, as well as operation without the clock for most features. The device also offers additional glue logic for general-purpose use. Available with a 3.5×3.5×1.2-mm footprint in a 36-pin, 0.5-ball-pitch package, the TC35892XBG costs $5.50 (10,000).

Toshiba America Electronic Components, www.toshiba.com/taec

EDN ADVERTISER INDEX

Company	Page
Actel Corp	51
Advanced Interconnections	62
Agilent Technologies	48
Allied Electronics	63
Altera Corp	17
Analog Devices Inc	19
Arrow Electronics	25
Astrodyne	C-3
austriamicrosystems AG	76
Avtech Electrosystems Ltd	85
Bias Power LLC	66
Bourns Inc	2
Central Semiconductor Corp	81
Digi-Key Corp	1
E-T-A Circuit Breakers	28
EMA Design Automation	C-4
ERNI Electronics	32
Fairchild Semiconductor	11
Intersil	4
	12, 37
Keithley Instruments Inc	33
Kemet Electronics Corp	55
Kepco Inc	64
LeCroy Corp	8
Linear Technology Corp	65
	67, 68
	77-78
LPKF Laser & Electronics	36
MathWorks Inc	35
Maxim Integrated Products	71
	73, 75
Memory Protection Devices	52
Mentor Graphics	43
Micrel Semiconductor	31
Micro Crystal	66
Microchip Technology	23
Mill Max Manufacturing Corp	84
Monolithic Power Systems	45
	47
National Instruments	13
	41
Pico Electronics	34
	46, 59
Power-One Inc	56
Radicom Research	85
Renesas Technology Corp	79
RFM	83
Samtec USA	53
Simlab Software GmbH	54
Sunstone Circuits Inc	61
Tadiran Electronic Industries	14
Tern	85
Texas Instruments	C-2
	3, 6
That Corp	52
Trilogy Design	85
Vicor	27
Xilinx Inc	21

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Temperature: your worst enemy?

DANIEL VASCONCELLOS

Many years ago, I was involved in an electromechanical project that included hydraulics, a microprocessor, custom chips, power circuits, software, dc motors, solenoids, and the like. I was responsible for overseeing the electronics and software that a supplier designed. Initial design and testing went well, but our team decided that we needed some early customer testing before starting production.

We wanted to continuously monitor and gather data on the operation and performance of the system. Therefore, I designed a field-data logger for the system that would communicate with the system via a serial-data link. We installed systems including these data loggers at a couple of customer sites and soon began getting reports of erratic system operation. Upon examination, we learned that one of the primary sensor signals that the system reported to the data logger was erratic. But, when we tested the systems, they all worked fine.

Nothing we did could make them operate erratically. The system needed to operate from −40 to +125°C outdoors and in harsh environments, but, in extensive lab testing at −40, 25, and 125°C, the testing showed no erratic operation. Production wasn't far away, and, if we couldn't resolve this problem, we would have to delay the start date, which would be expensive.

One of the supplier's technical engineers had seen some erratic system operation. So we decided to do additional lab testing with a temperature sweep of 5°C steps from −40 to +125°C and with some of the complaining customers' data loggers connected to the systems. The data loggers immediately showed the same erratic sensor signal and system operation.

We concluded that the system electronics were corrupting the signals. Examining the data from the data loggers showed what time of day the erratic operation was occurring. We compared the erratic-incident time with the lab-test results and found an interesting phenomenon: The erratic operation was occurring over a narrow temperature range, inconsistent from system to system. One system showed the problem at 40 to 80°C, and another showed it at 60 to 90°C. Each system that displayed the problem had a different starting temperature and a somewhat different range; no problems were occurring at the nominal ambient of 25°C or at the temperature extremes. We quickly narrowed the culprit down to the signal-processing chip in the system's electronics.

The custom-built IC had both positive- and negative-temperature-coefficient components that determined the sensor-signal thresholds and hysteresis. Because the internal component's temperature coefficients were not matched, at certain temperatures over a narrow range, the signal threshold would rise to or slightly above the sensor's output, and the needed signal hysteresis would disappear. We redesigned this custom IC and expedited production. We barely made it into production on time, but we had no further problems.

We learned a number of lessons and had a bit of luck. We designed the system with the ability to report incoming and internal signals and status, without which the problem would have taken a lot longer to detect and fix. We opted for early customer testing well ahead of production. The biggest lesson we learned was that you must monitor temperature-sensitive components, parts, or subsystems with temperature-sweep testing over the full specification range. EDN

Consultant Clark Robbins is a software-application engineer. Like him, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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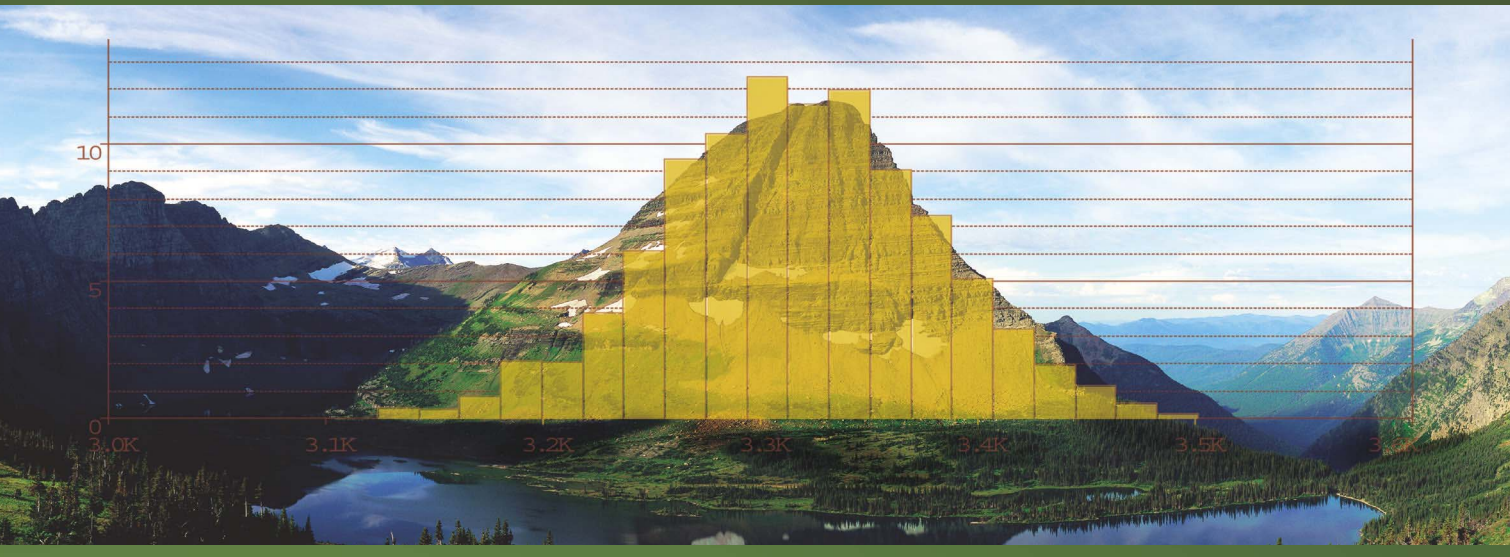

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